

Model Name: GA-H87-D3HP

1.0

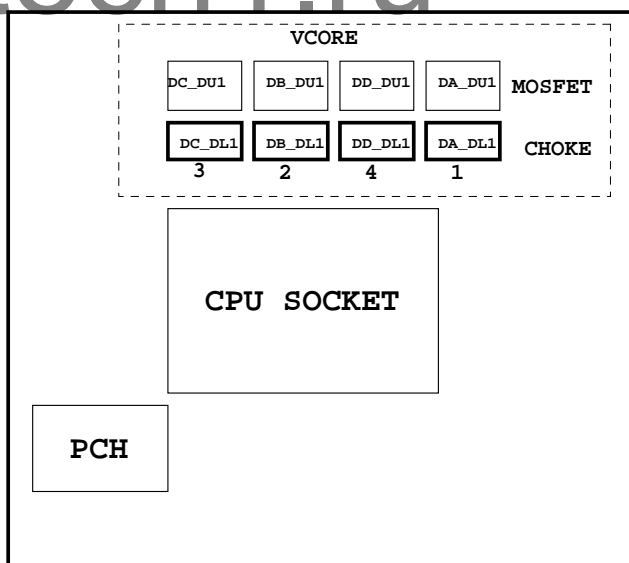
SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE PWM_IR3564a
24	VCORE+DDR PWM IR3553+IR3598
25	ME POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	LAN INTEL i217
32	DVI
33	HDMI , R_USB30
34	TABLE LIST
35	
36	
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38	
39	
40	

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GA-H87-D3HP

Component value change history

Data	Change Item	Reason
0.1-0925	E-BOM	
	1. Z77-D3H改為削光黑PCB, slots同原本削光黑機種配色, CPU socket線黑	
	2. 8 series IR digital power PWM因Intel spec change, 須改用b版 (必須發行Firmware)	
	3. H77-D3H 注意上H87 chips, 上ME power, 咖啡黑機種配色, CPU socket standard, clock buffer要上	
	3. H77-D3H GPIO37 需Pull up to 3VDUAL	
0.2	1. Load-line DAR47 2.06K --> 2.37K , DAR46/50 1.4K --> 1.6K , DAC17 150P --> 100P	
	2. N_-LAN_WAKE NR60 8.2K/4 --> 1K/4/1	
	3. DA_DUI, DB_DUI, DD_DUI, DC_DUI 10IFB-403553-01R --> 0TA1-603551-00R	
	4. DDR CHOKE阻值調整	
	5. CPU SOCKET + RM 要用新料號?	
0.2B	1. 確定Power stage用料: IR3553 or IR3550 or 3551?	
	2. GPIO8 "NR136"不上	
	3. Add +12V排阻 RN2-RN6	
0.2C	1. HU1 , HU2 level shifter change to NXP	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
	3. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak	
1.0	1. PCIE X16 patch reset circuit 怎麼上?	
	2. Prochot是否只上一組	
	3. PCH_HS & MOS_HS change new 料號	
	4. 因DII 2222禁用, 注意Z87-D3H試產時用Panjit 2222是否可用(BOM已內建)	
	5. HDMI/DVI change to NXP level shifter	
	6. CHECK 5VSB保護線路是否上件	
Z87-D3HP		
1.0A	1. 5VDUAL OVP --> 5VSB OVP	
	2. Remove 全成信PCB	
1.0B	1. Remove DAJP1	
	2. HR29 3.09K --> 3.3K	
	3. USB3.0 HUB add RT9018	

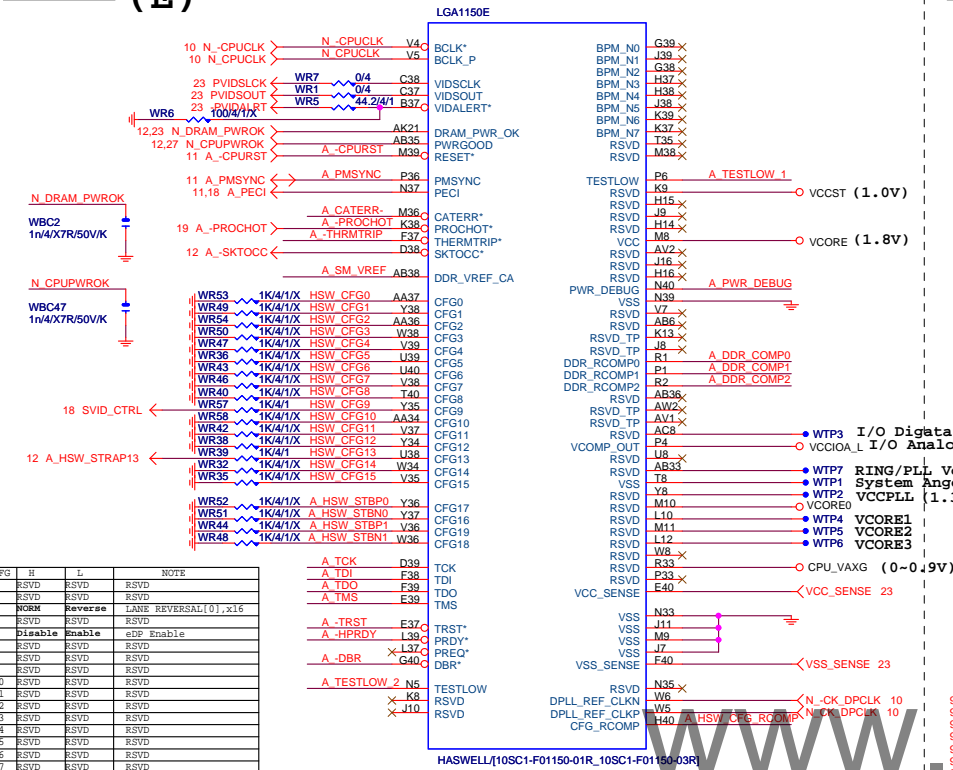
Circuit or PCB layout change

DATE	Change Item	Reason
0.1	E-BOM	
0.2	1. U8 pin3加粗40mils 2. Update LAYOUT NEW RULE for四層板 3. MDA6線長T型要繞等長 4. N_GPIO37 pull up VCC3 --> 3VDUAL 5. CPU Thertrip CPU_VTT --> VCC1_05_PCH 6. 確認 R/G/B ESD擺放位置 7. Add PCIE X16 reset patch circuit 8. PCIE signal by group 成對走 9. VIN0 --> VCORE0 , VIN5 --> VCORE 10. CS 1pin --> 2pin 11. 後窗部份鋪銅會挖 + 字處理 12. Add MA_DR8 , MA_DC8單獨下地 13. add VTT_PWRGD control circit 14. Update F_PANEL footprint "H2X10PANEL-3" 15. NR132跟NC59 layout位置交換 16. Add DS_ME GP67 control 17. Q6位置靠近 PWM power control pin 18. WR59 change to "R0204-2" 19. 文字面 "DualBIOS" , 改為" Dual UEFI BIOS" , Add "Intel GbE LAN" 20. MAU2 REF "GND" 21. DDR Choke ML1, ML2 1.2uH/20A --> 0.8uH/35A	
0.21	1. AUDIO SPDIF-IN CR77 "0402-2" FOR short protection 2. add AUDIO ON/OFF PLAYER 3. Change PCIE X1/PCIE X4 CLK 4. Update F_PANEL footprint 5. CPU VRIN OV IO_GP81 --> IO_GP21	
0.3	1. PWM MOSFET修改 IR3564B + power stage 改成 IR3564B + IR3535 + power pak (Cancel)	
1.0	1. 0 ohm --> short pad 2. 簡化CPU Config setting 3. Remove "BIOS_PH" & "M_BIOS socket" & "CS" pin 4. 注意Slot和後窗正面有做十字Thermal處理 5. NBC65移靠近PCH 6. Add R700-R702 for FAN short protection 7. PWR_LED 改為IO_GP65 8. VTT_PWRGD Update 9. N_GPIO37 pull-up to VCC3 10. +12V RN2-RN6 & VCC/VCC3/5VSB dummy load 排阻 11. DDR_15V H/W monitor detect 改從 DDR slot 拉回 12. 5VSB AD1要過 NET 13. DDR VIN 間隔拉開 , 背板GATE往上移 14. Add DDR_15V dummy load 15. 5VSB/5VDUAL OVP protection 16. 預留N_PCH_DPWROK 控制線路	
Z87-D3HP-0.1	1. add USB3.0 Hub	

Z87-D3HP-1.0 1. DART2改成R0402-2(靠近DD_DUI) , DART4改成R0603-RH(放在DART2左邊) , RS1改成R0402-2
2. Add DAR82 For MOSFET "PHSFLT-" protect

Gigabyte Technology		
Title BOM & PCB MODIFY HISTORY		
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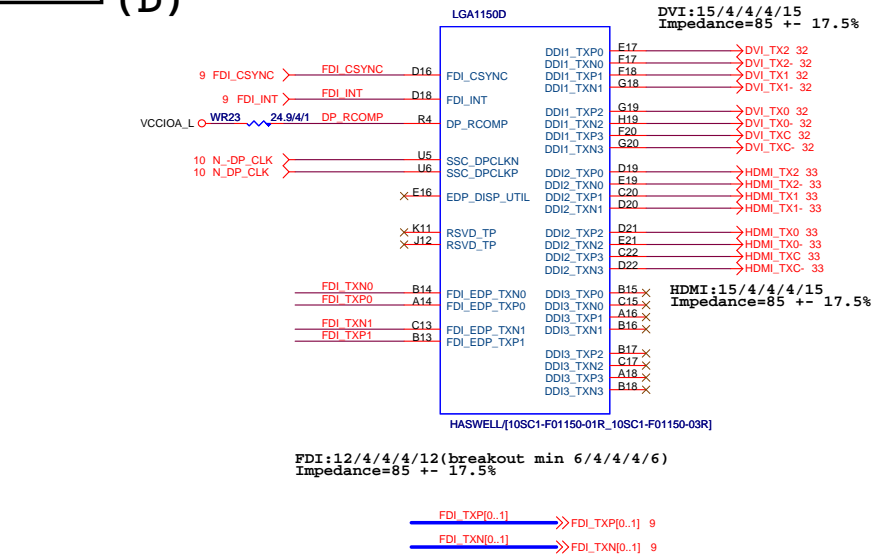
LGA1150 (E)



CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2x8
0	1	RSVD
0	0	X8, X4, X4

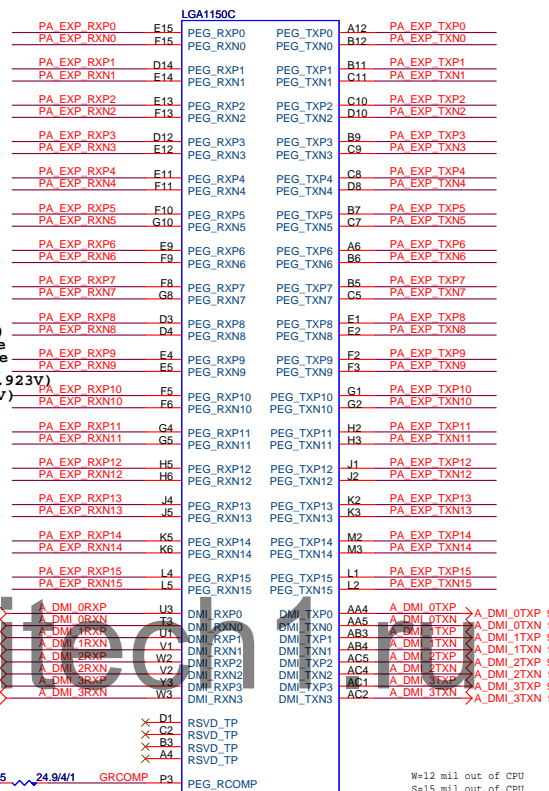
G 0-17 all internal PULL-UP

LGA1150 (D)

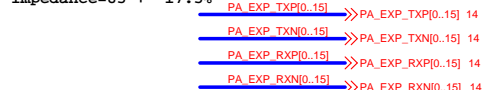


LGA1155 (C)

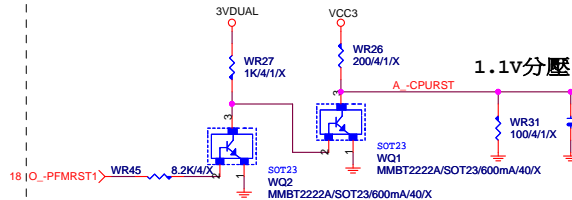
PCIEEX16:20/5/4/5/20(breakout min 10/4/4/4/10)
Impedance=80 +- 17.5%



DMI:12/4/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%



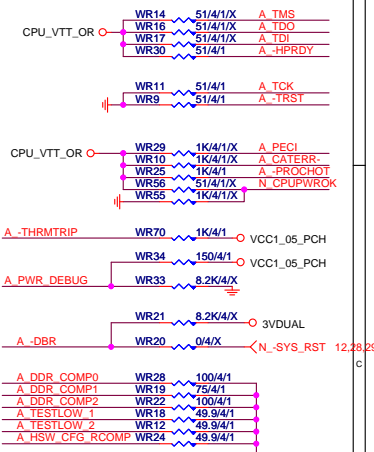
-CPURST



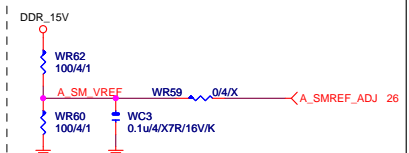
CPU SVID



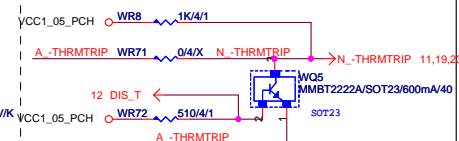
CPU	PU/PD
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SM REF



THRMTRIP DISABLE



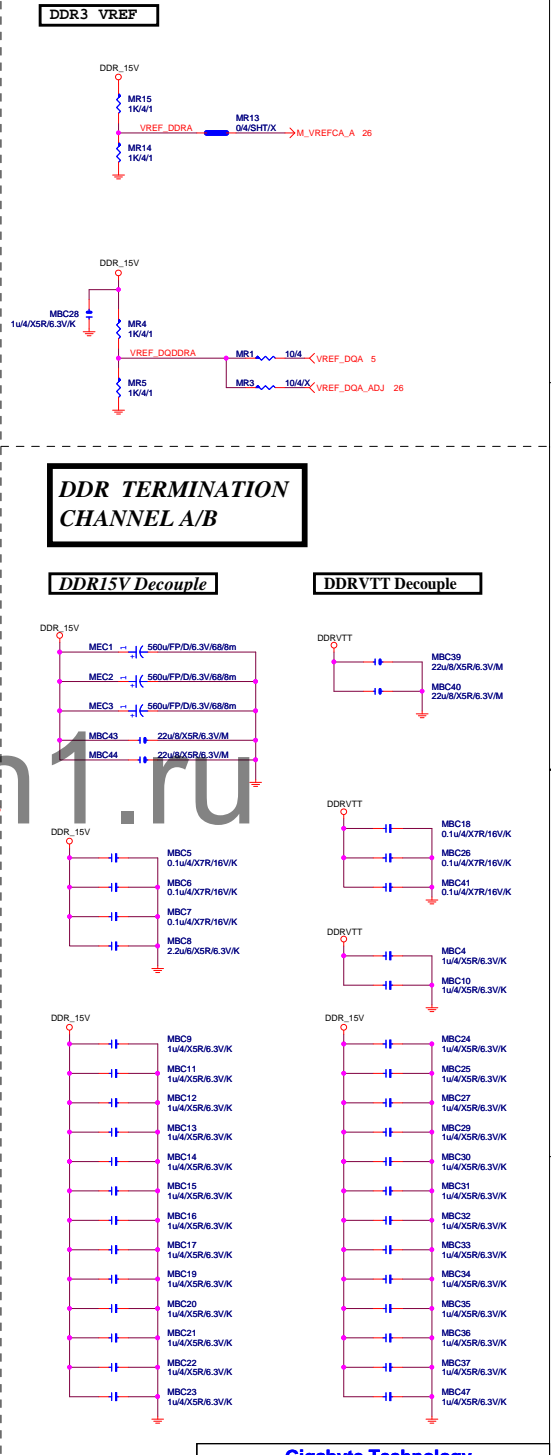
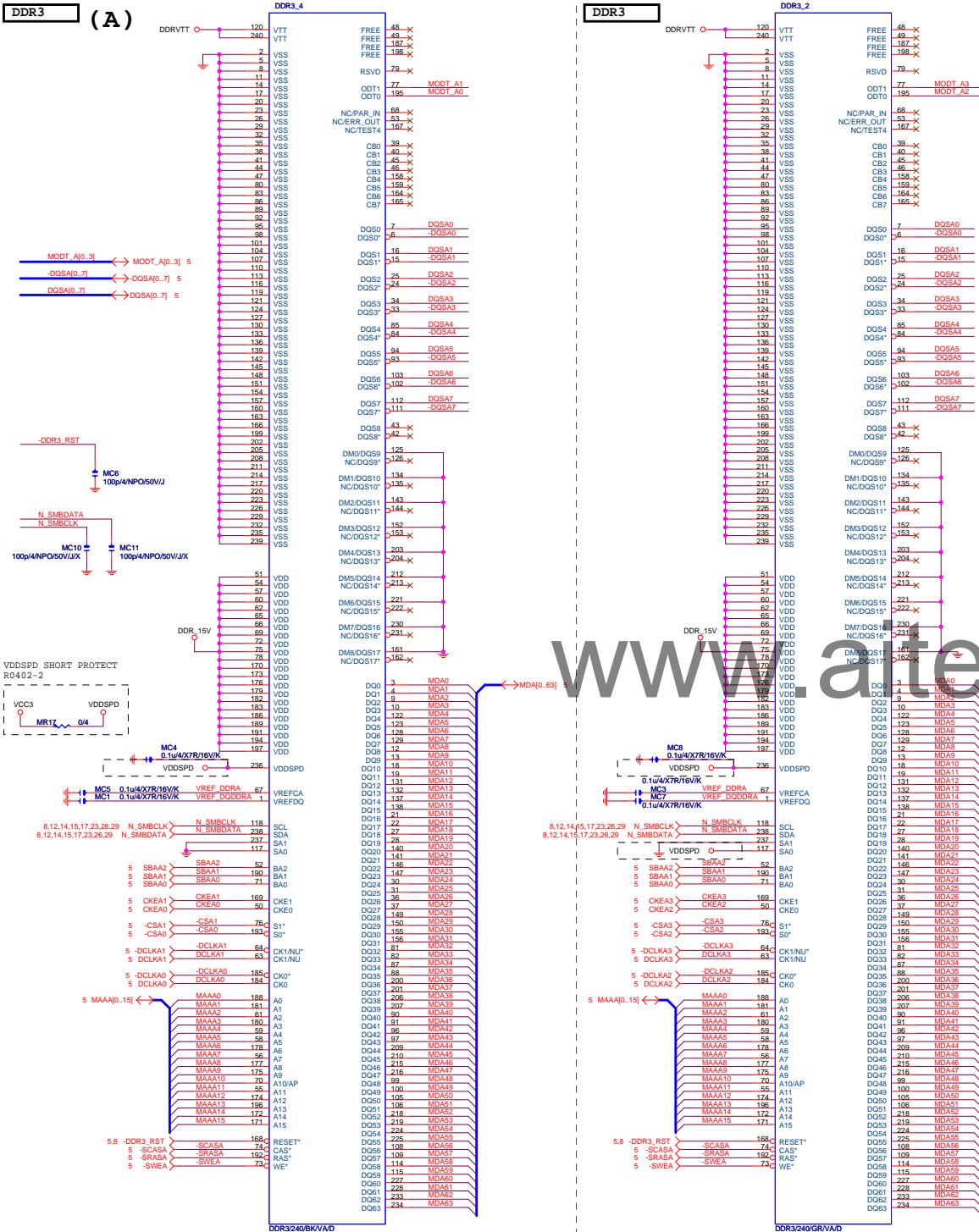
Title			
CPU LGA1150-B			
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(F, J)



GA-H87-D3HF

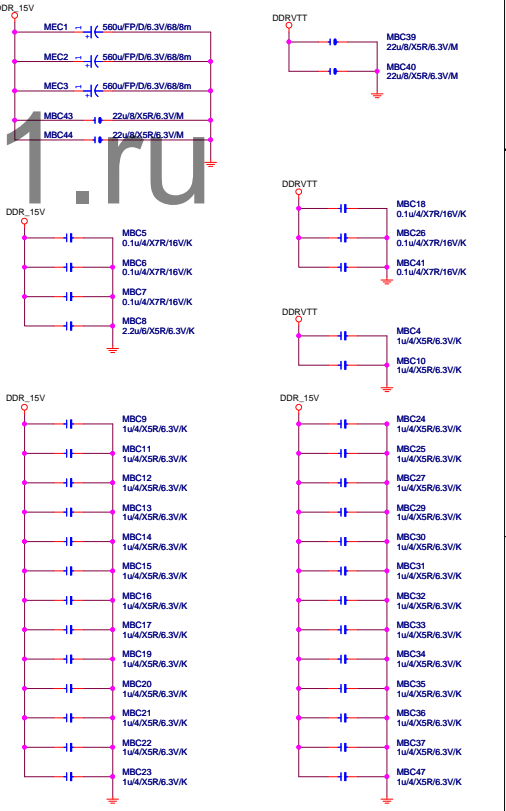
Custom	CA Net 2011			1.0
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DDR TERMINATION CHANNEL A/B

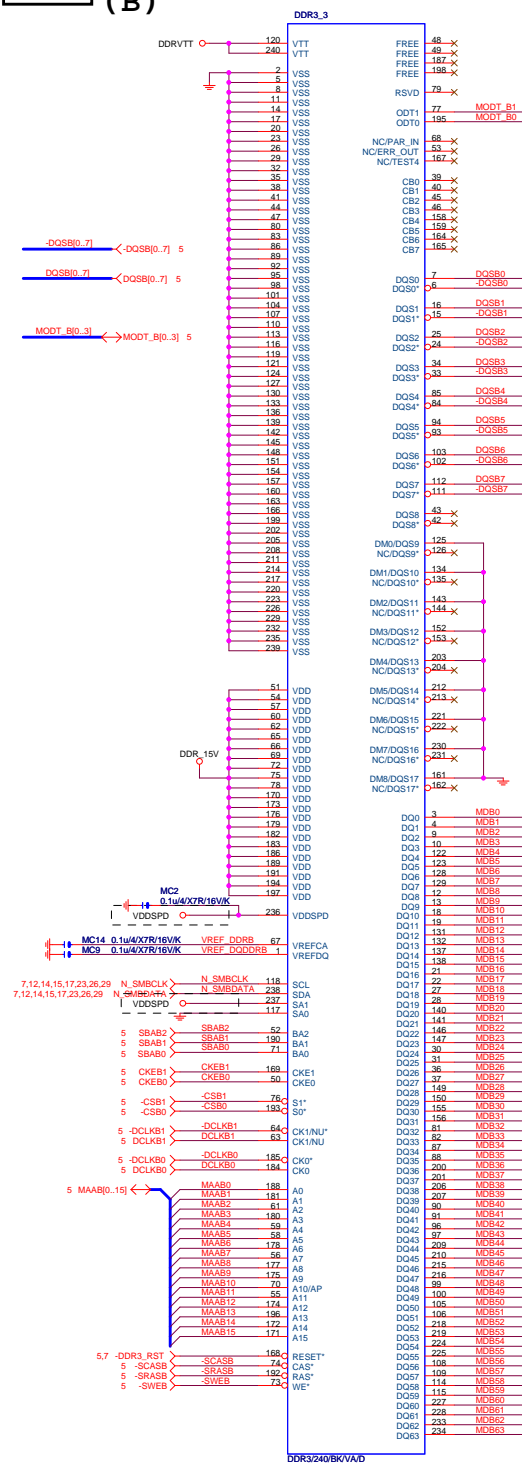
DDR15V Decouple

DDRVTT Decouple



DDR3

(B)



PCH (B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

4 A DMI_0TXN A DMI_0TXP L24
4 A DMI_0TXP A DMI_0TXP K24
4 A DMI_0RXN A DMI_0RXN C20
4 A DMI_0RXP A DMI_0RXP B20
4 A DMI_1TXN A DMI_1TXN G24
4 A DMI_1TXP A DMI_1TXP H24
4 A DMI_1RXN A DMI_1RXN D24
4 A DMI_1RXP A DMI_1RXP B21
4 A DMI_2TXN A DMI_2TXN F26
4 A DMI_2TXP A DMI_2TXP G26
4 A DMI_2RXN A DMI_2RXN B22
4 A DMI_2RXP A DMI_2RXP C22
4 A DMI_3TXN A DMI_3TXN K26
4 A DMI_3TXP A DMI_3TXP L26
4 A DMI_3RXN A DMI_3RXN A24
4 A DMI_3RXP A DMI_3RXP B24

VCC1_5_PCH NR50 7.5K/4/1 DMI_COMP B19
W=8 mil out of PCH NR40 7.5K/4/1 PCIE_COMP C13
S=15 mil to other signals CK-SRCLK_PCH CK-SRCLK_PCH G22
CK-SRCLK_PCH CK-SRCLK_PCH F22

ITE8892 PCI Bridge
PCIEX1 port1 15 PI_PCIE_IN1 L14
15 PI_PCIE_IP1 K14
15 PI_PCIE_TN1 B12
15 PI_PCIE_TP1 B11
15 PJ_PCIE_IN2 F14
15 PJ_PCIE_IP2 D11
15 PJ_PCIE_TN2 C11
15 PJ_PCIE_TP2 F11
LAN AR8161 31 LB_ML_IN H11
31 LB_ML_IP B9
31 LB_ML_ON A9
31 LB_ML_OP J11
16 G_PCIEBIN L11
16 G_PCIEBIP B8
16 G_PCIEBON C8
16 G_PCIEBOP G9
PCIEX4 port1 15 PE_PCIE_IN1 E9
15 PE_PCIE_IP1 E7
15 PE_PCIE_TN1 A7
15 PE_PCIE_TP1 F7
15 PF_PCIE_IN2 H7
15 PF_PCIE_IP2 D2
15 PF_PCIE_TP2 K6
PCIEX4 port2 15 PG_PCIE_IN3 K6
15 PG_PCIE_IP3 G3
15 PG_PCIE_TP3 G5
PCIEX4 port3 15 PH_PCIE_IN4 J3
15 PH_PCIE_IP4 H2
15 PH_PCIE_TP4 H1

電容放靠近 Device & PCI-E Slot

PCIEX1:15/4/4/15 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

PCH_PCIE, DMI 15/4/4/4/15

usb2.0 12/5/7/5/12
usb3.0 20/5/7/5/20

PCH (F)

USB3.0 : 20/5/7/5/20 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

28 PCH_USB3_RXN0 F20 USB3_RXN_0
28 PCH_USB3_RXP0 G20 USB3_RXP_0
28 PCH_USB3_TXN0 B18 USB3_TXN_0
28 PCH_USB3_TXP0 C18 USB3_TXP_0
28 PCH_USB3_RXN1 G18 USB3_RXN_1
28 PCH_USB3_RXP1 H18 USB3_RXP_1
28 PCH_USB3_TXN1 B15 USB3_TXN_1
28 PCH_USB3_TXP1 B16 USB3_TXP_1
34 PCH_USB3_RXN4 K20 USB3_RXN_4
34 PCH_USB3_RXP4 L20 USB3_RXP_4
34 PCH_USB3_TXN4 D15 USB3_TXN_4
34 PCH_USB3_TXP4 C15 USB3_TXP_4
36 PCH_USB3_RXN5 L18 USB3_RXN_5
36 PCH_USB3_RXP5 K18 USB3_RXP_5
36 PCH_USB3_TXN5 B14 USB3_TXN_5
36 PCH_USB3_TXP5 A14 USB3_TXP_5

VCC3 NR62 8.2K/4 AK28 TACH6_GP70
NR63 8.2K/4 AT34 TACH7_GP71

H87/S[10HB1-030H87-10R]
FDI_TXP0..1 FDI_TXP0..1 4
FDI_TXN0..1 FDI_TXN0..1 4

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

CK SRCLK_PCH NR89 8.2K/4
CK-SRCLK_PCH NR88 8.2K/4
Mount for integrated clock Generation Mode

CK_DOTCLK NR92 8.2K/4
CK-DOTCLK NR91 8.2K/4
NR92 short to GND in non graphic SKU

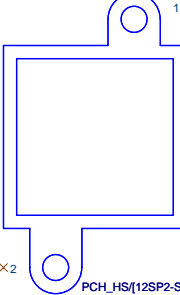
PCH (J)

AT1 VSS_NCTF TP22 U11
AT41 VSS_NCTF TP23 U10
AU1 VSS_NCTF TP21 AJ14
AV1 VSS_NCTF TP20 AK14
AV2 VSS_NCTF TP14 K34
AV40 VSS_NCTF TP15 K33
AV41 VSS_NCTF TP12 AH24
AW2 VSS_NCTF TP10 L16
AW40 VSS_NCTF TP11 K16
B40 VSS_NCTF TP9 AM34
B41 VSS_NCTF TP3 R12
C41 VSS_NCTF TP4 N12
D1 VSS_NCTF TP1 L22
D41 VSS_NCTF TP2 K22
TP5 R4
TP6 K5
TP7 P5
TP8 L5
VSS AC31
VSS AF3
VSS AV21

H87/S[10HB1-030H87-10R]

PCH H/S

PCH_HS



PCH_HS[12SP2-S06012-11R_12SP2-S06012-12R_12SP2-S06012-13R]

USB TABLE

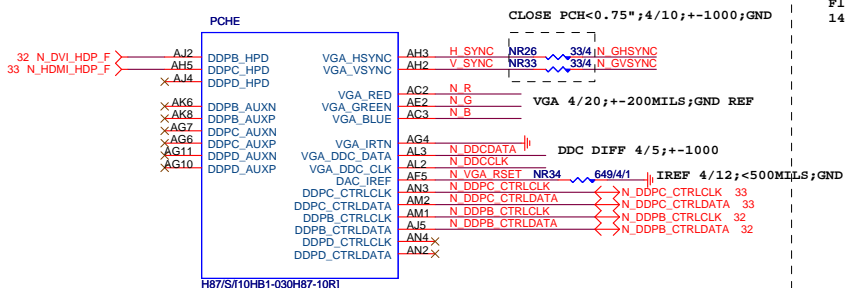
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

Gigabyte Technology

Title PCH FDI,DMI,USB ,PCIE		
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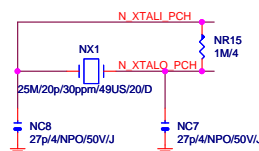
PCH (E)



VGA DISABLE	
R,G,B	NC OR GND
IRTN / IREF	GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA	NC
POWER VCCADAC(AF2), VCCADACBG(AE1)	GND

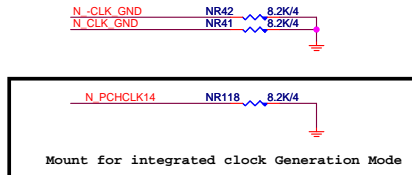
PCH (G)

Flex1,2,3,4 : 14/24/33/48MHz

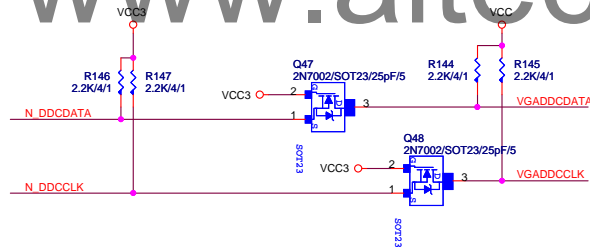


Differential Clock: 15/4/6/4/15
Impedance=90 +- 15%

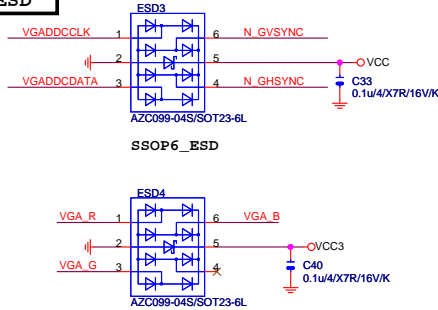
PCH CLK PD



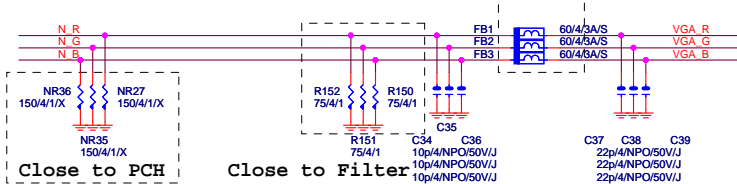
VGA DDC



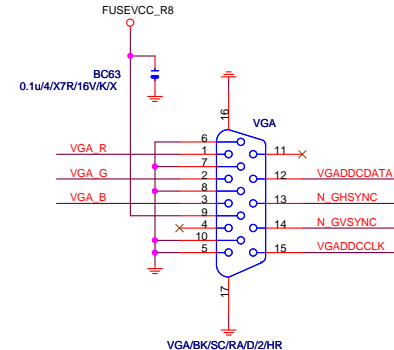
VGA ESD



VGA DDC



VGA CONNECTOR

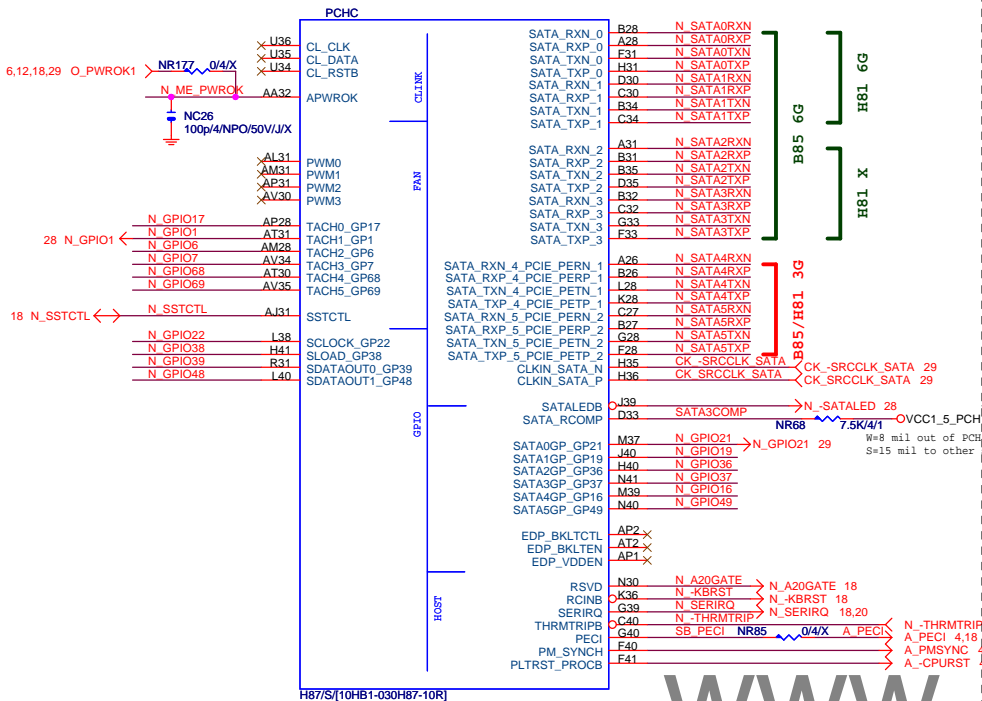


Gigabyte Technology		
Title		
PCH DISPLAY ,CLK BUFFER		
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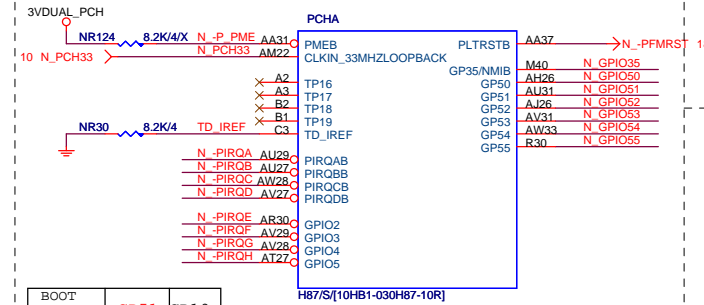
PCH

(C)

SATA3 : 20/4/4/20 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%



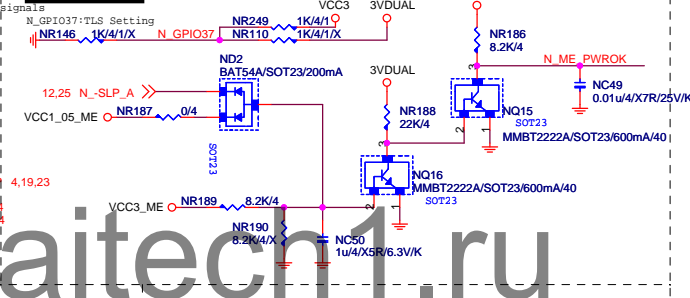
PCH (A)



BOOT DEVICE	GP51	GP19
LPC	0	0
SPI	1	1

Default int pull up on GP51,
Default SPI boot devices

ME PWROK N_GPIO37 For H87/B85



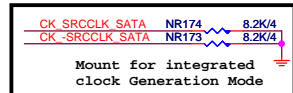
GPIO38 Ctrl

MFG Mode

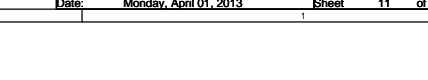
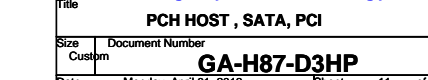
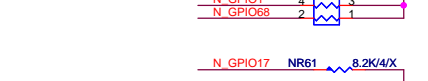
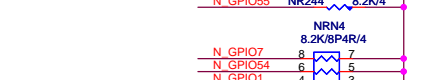
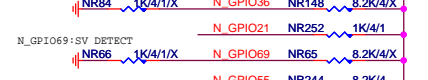
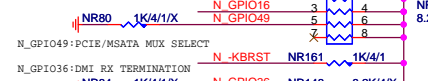
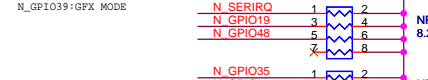
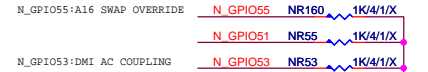
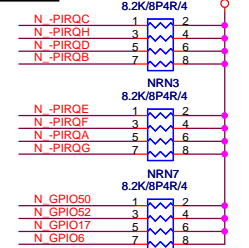
N_GPIO38 : Lo --> Enable
Hi --> Disable

12 N_GPIO60 NR184 8.2K/4

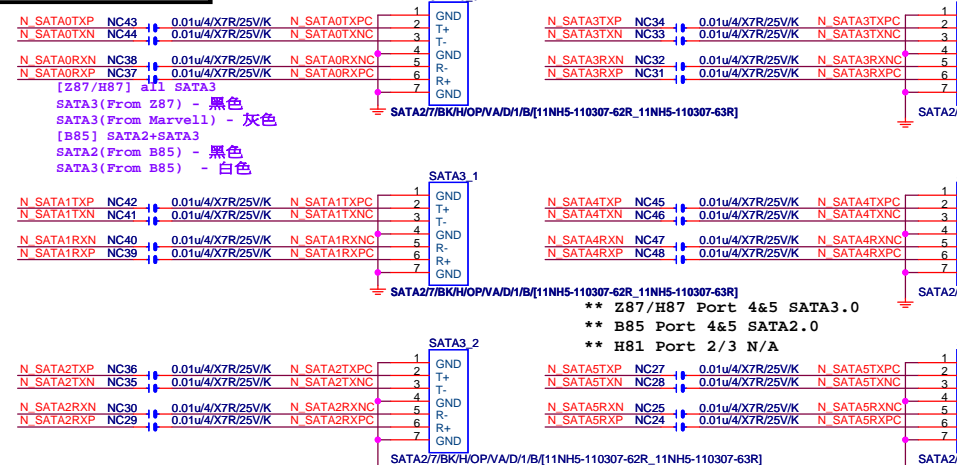
PCH CLK PD



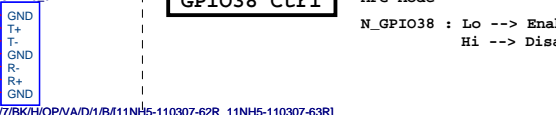
PCH PU/PD



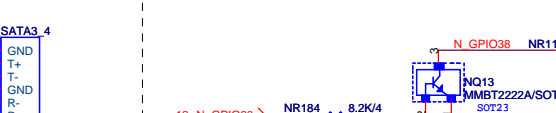
SATA3 CONNECTOR



SATA3_0



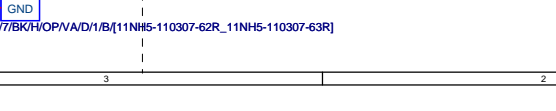
SATA3_1



SATA3_2



SATA3_3



SATA3_4



SATA3_5

Gigabyte Technology

PCH HOST , SATA, PCI

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Rev 1.0

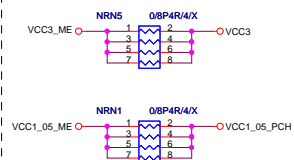
GA-H87-D3HP

PCH (I)

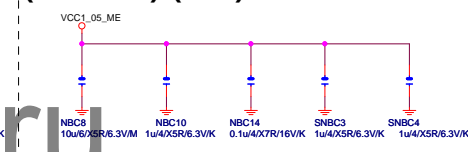


SHT PWR

CAP



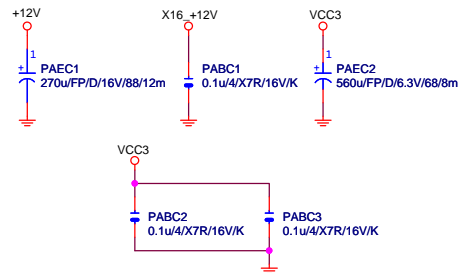
(1.05V) (x5)



(1.05V)(x2) (3.3V) (x2)

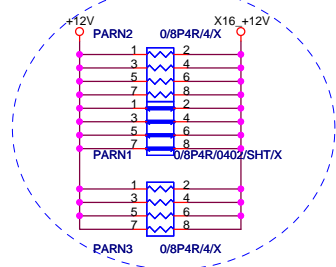


PCIEX16 CAP



PCIEX16 PROTECT SHT

```
+12  protect
short-wire test
```



PCIEX16	AC	CAP
---------	----	-----

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAc7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC3	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

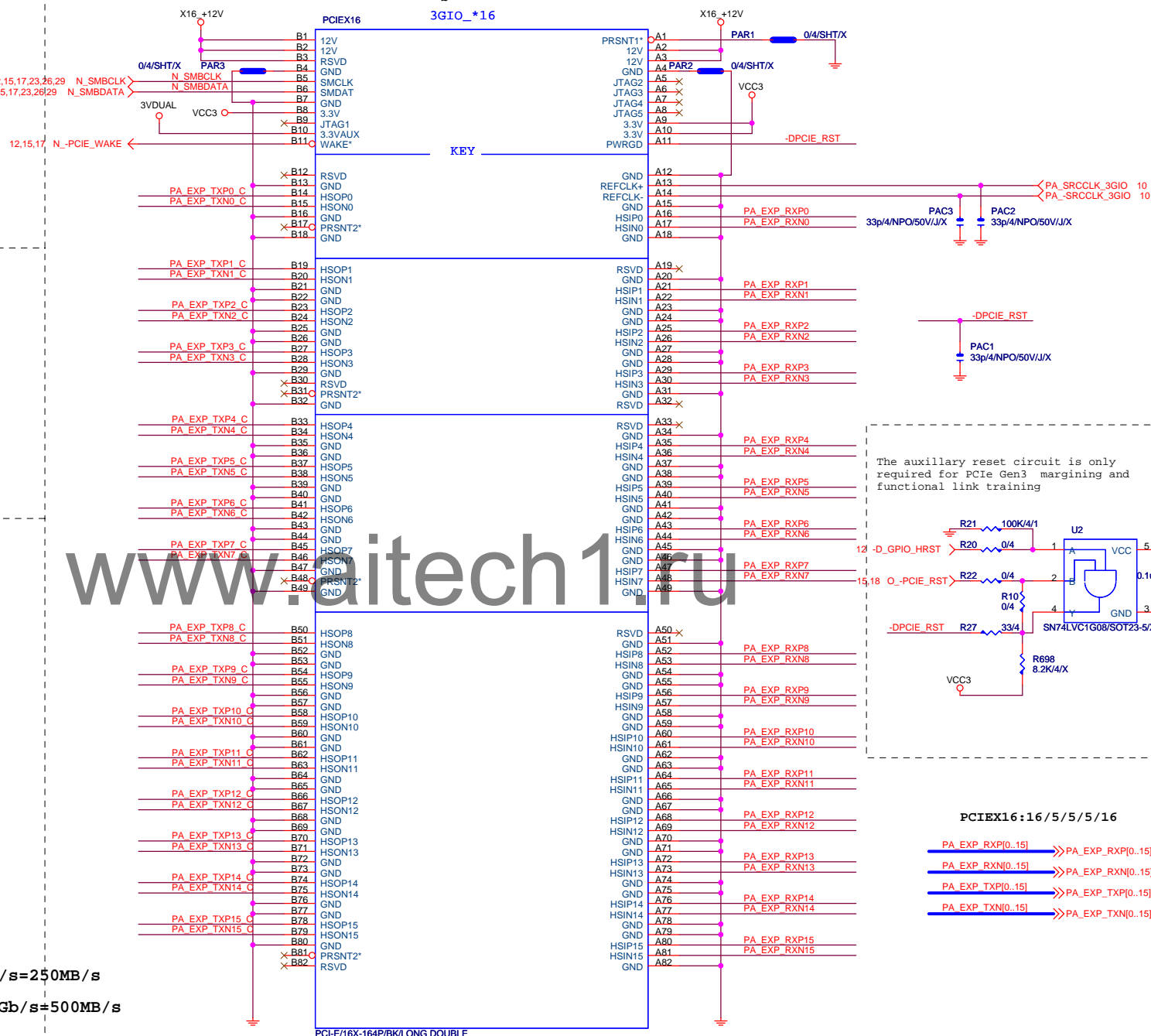
PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCIEX16 SLOT

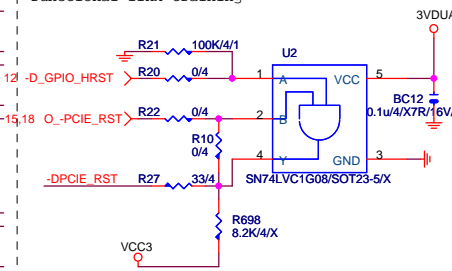
PCIESLOT-164DN-Q



```

- | The auxillary reset circuit is only
- | required for PCIe Gen3  margining and
- | functional link training

```

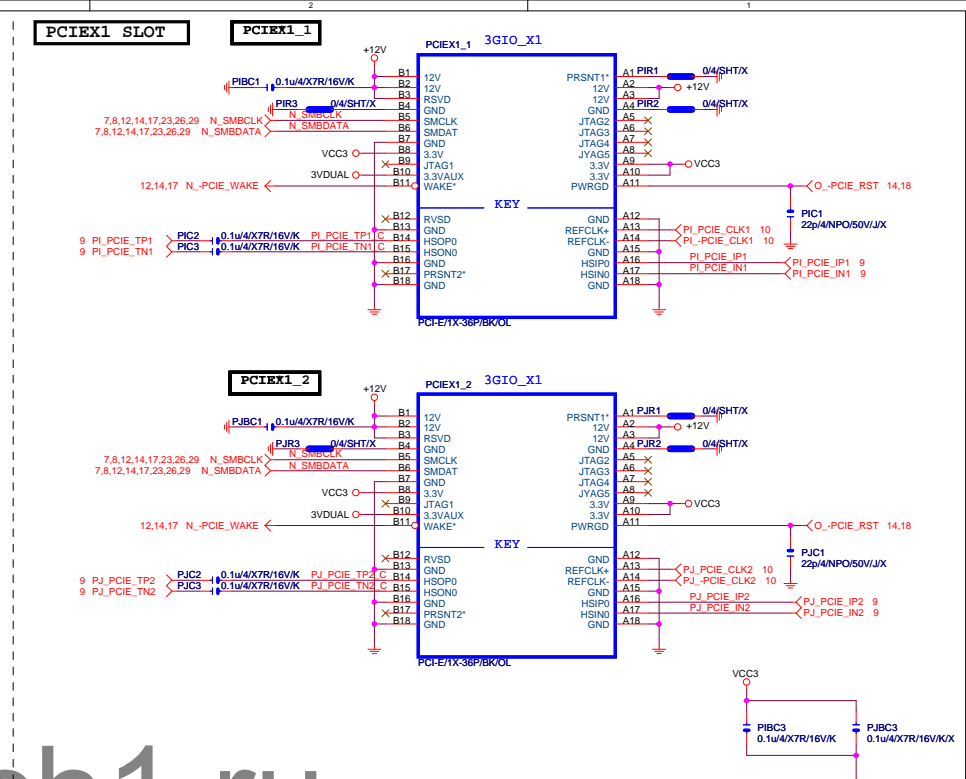
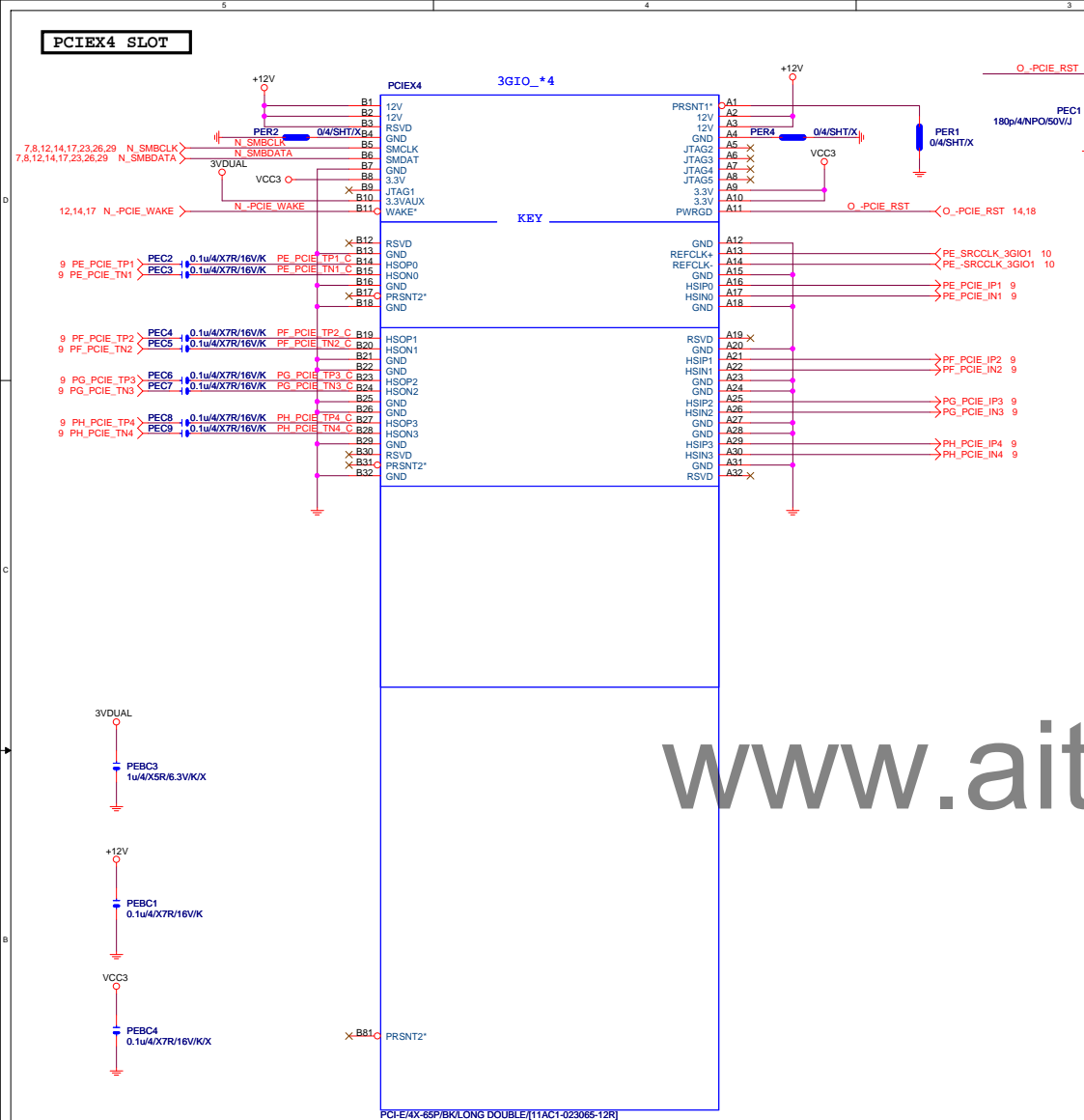


PCIEX16:16/5/5/5/16

```

PA_EXP_RXP[0..15]    >> PA_EXP_RXP[0..15] 4
PA_EXP_RXN[0..15]    >> PA_EXP_RXN[0..15] 4
PA_EXP_TXP[0..15]    >> PA_EXP_TXP[0..15] 4
PA_EXP_TXN[0..15]    >> PA_EXP_TXN[0..15] 4

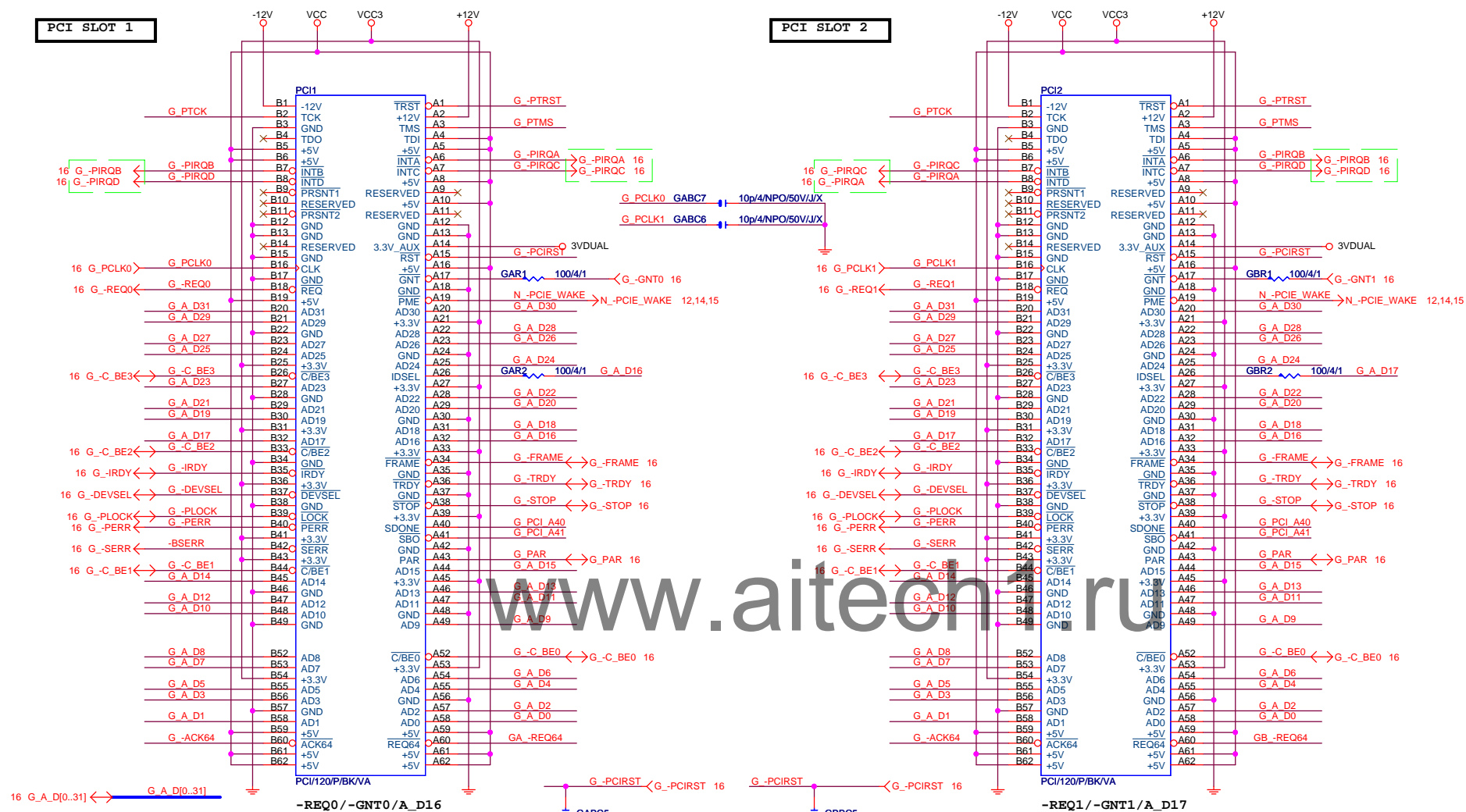
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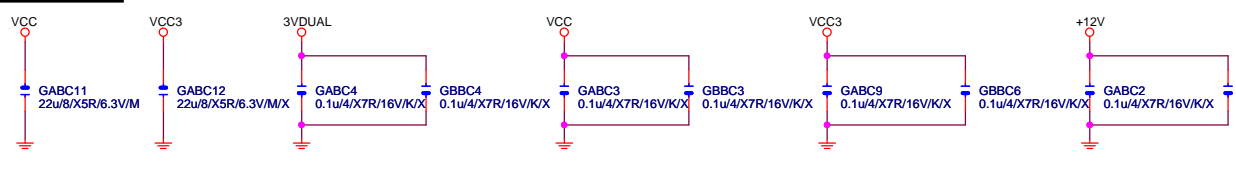
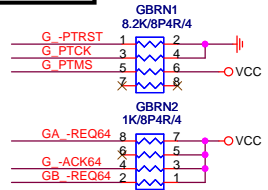
PCI SLOT 1

PCI SLOT 2



PCI PU

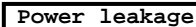
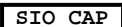
PCI CAP



PCI SLOT 1&2

Size	Document Number	Rev
Custom	GA-H87-D3HP	1.0
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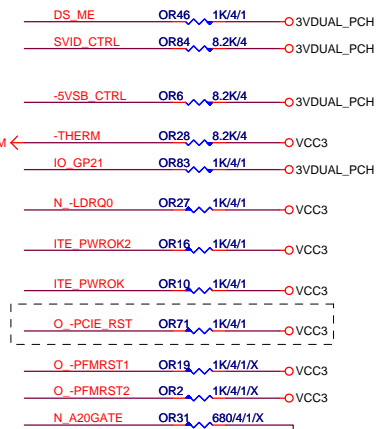
IT8728F NOTE

DUAL BIOS OPT STRAPPWR SHT

For 8728 EUP function

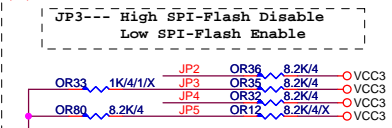


SIO	PU
-----	----



```
Hi :Disable WDT
Lo :Enable WDT to rest PWROK
```

2 SIO STRAP



```
JP5:N\A FOR 8728 DX
JP5:PULL DOWN FOR 8728 EX
anti-surge enable
```

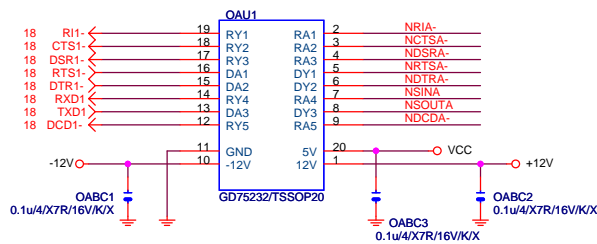
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EUP control detect

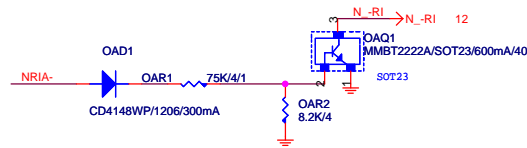
```

JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h
	0 0	The default value of EC Index 63h/6Bh/73h is 40h

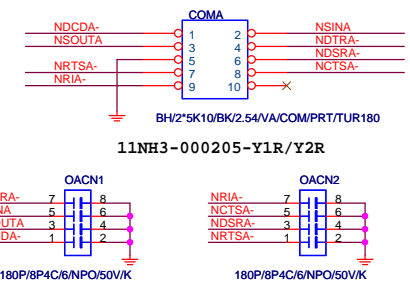
COMA



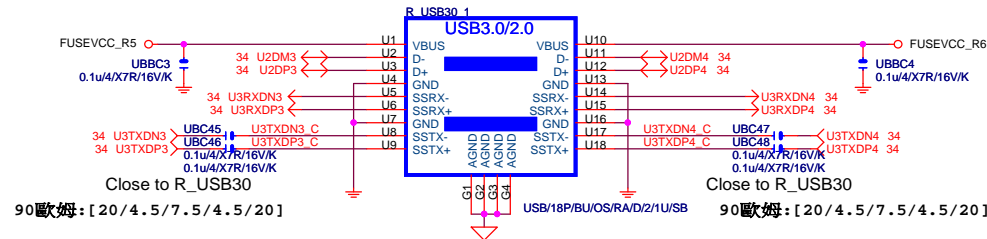
COM RI



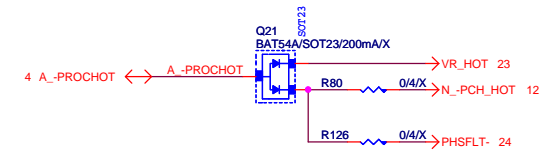
COM BUFFER



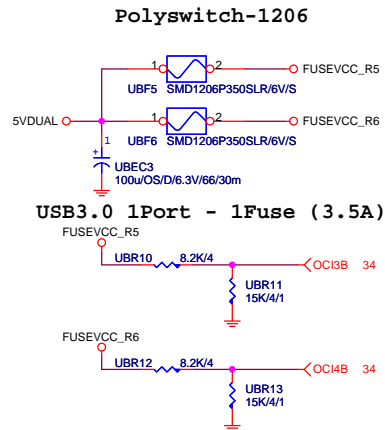
USB30_20 CONNECT



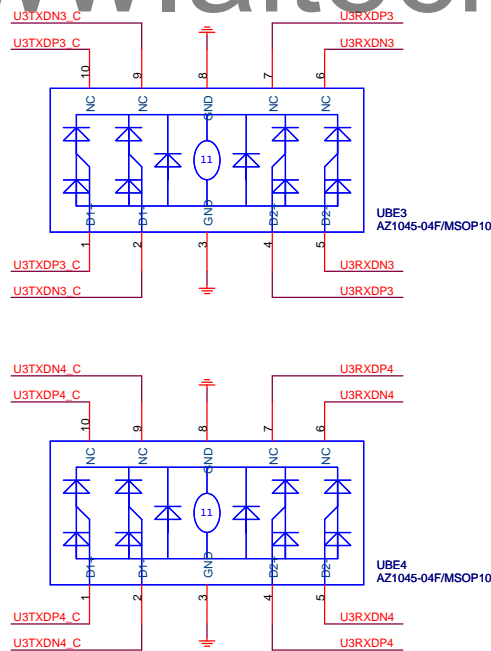
-PROHOT



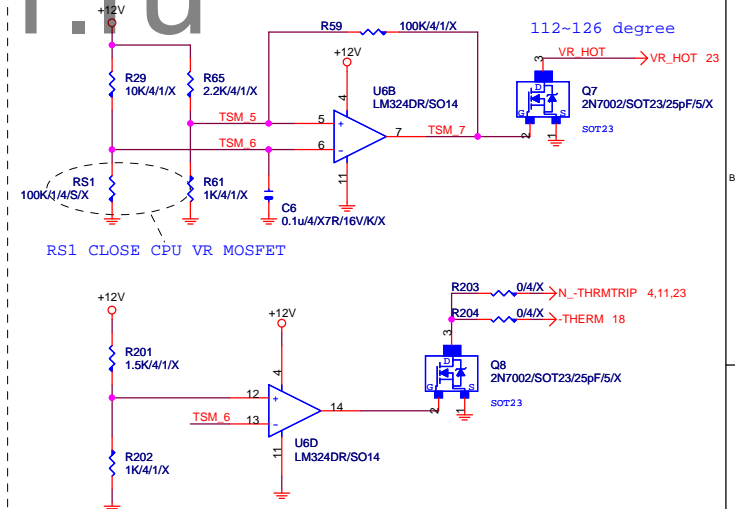
USB30 PWR



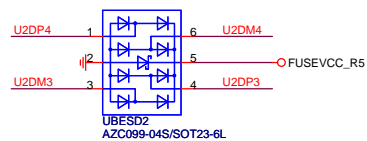
USB30 ESD PROTECT



-PROHOT



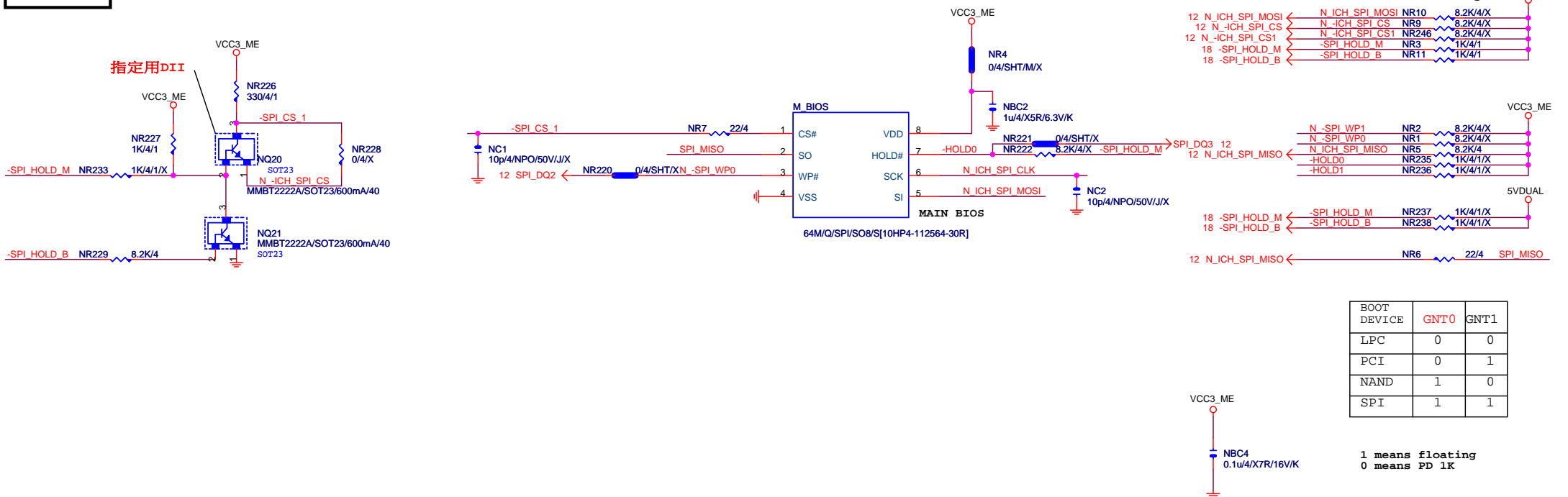
USB20 ESD PROTECT



Gigabyte Technology

Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custom		GA-H87-D3HP	
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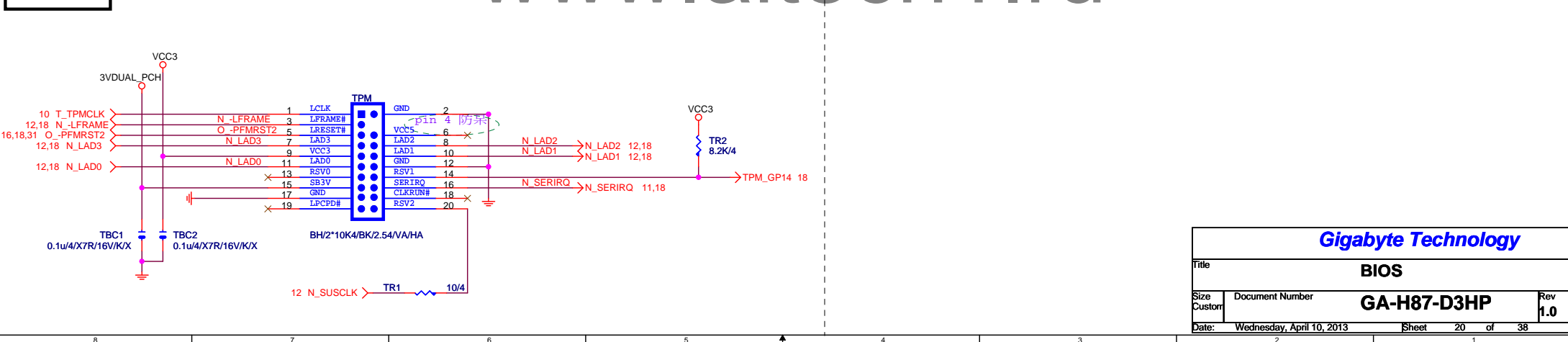
DUAL BIOS



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

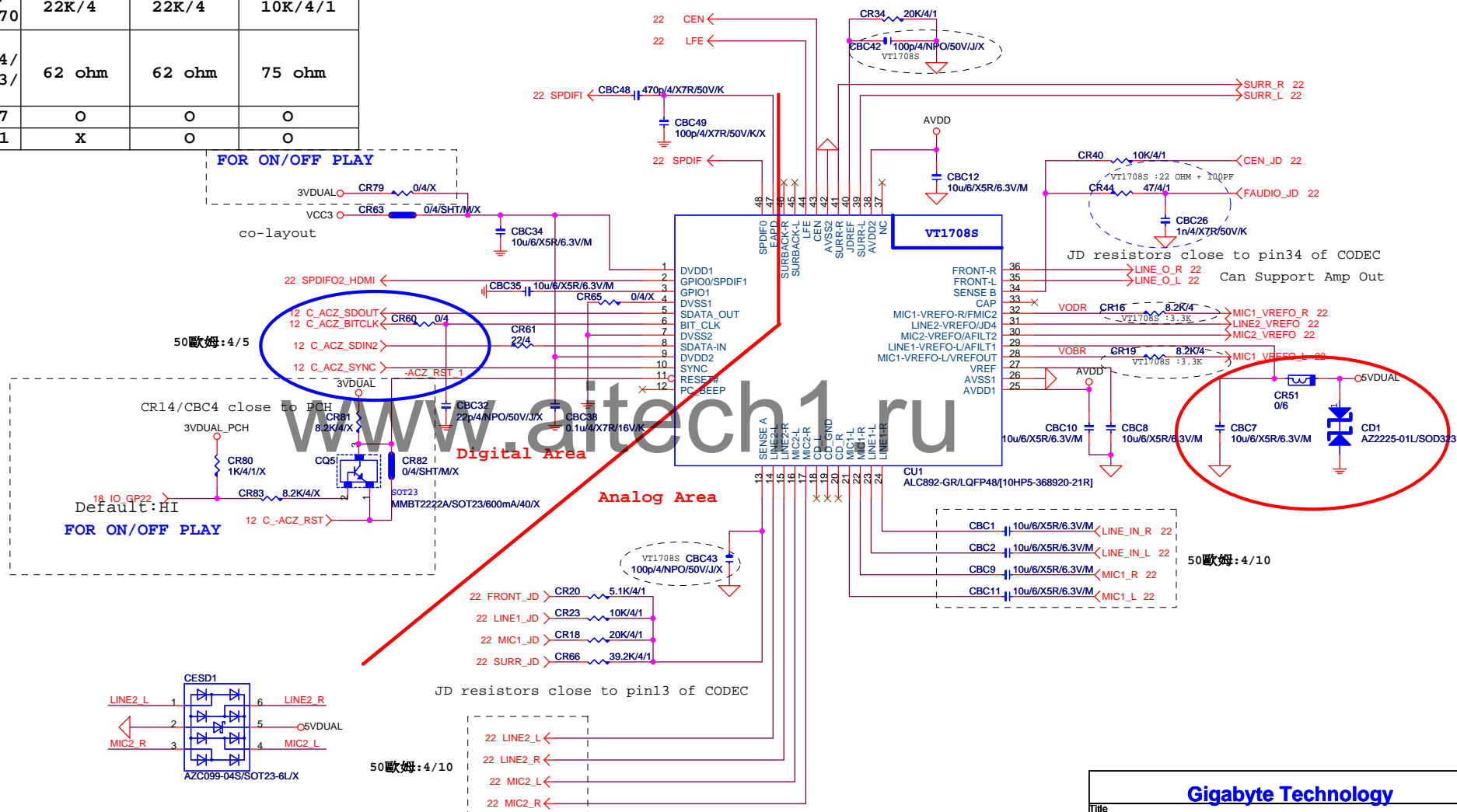
TPM CONNECT

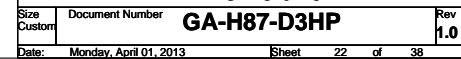


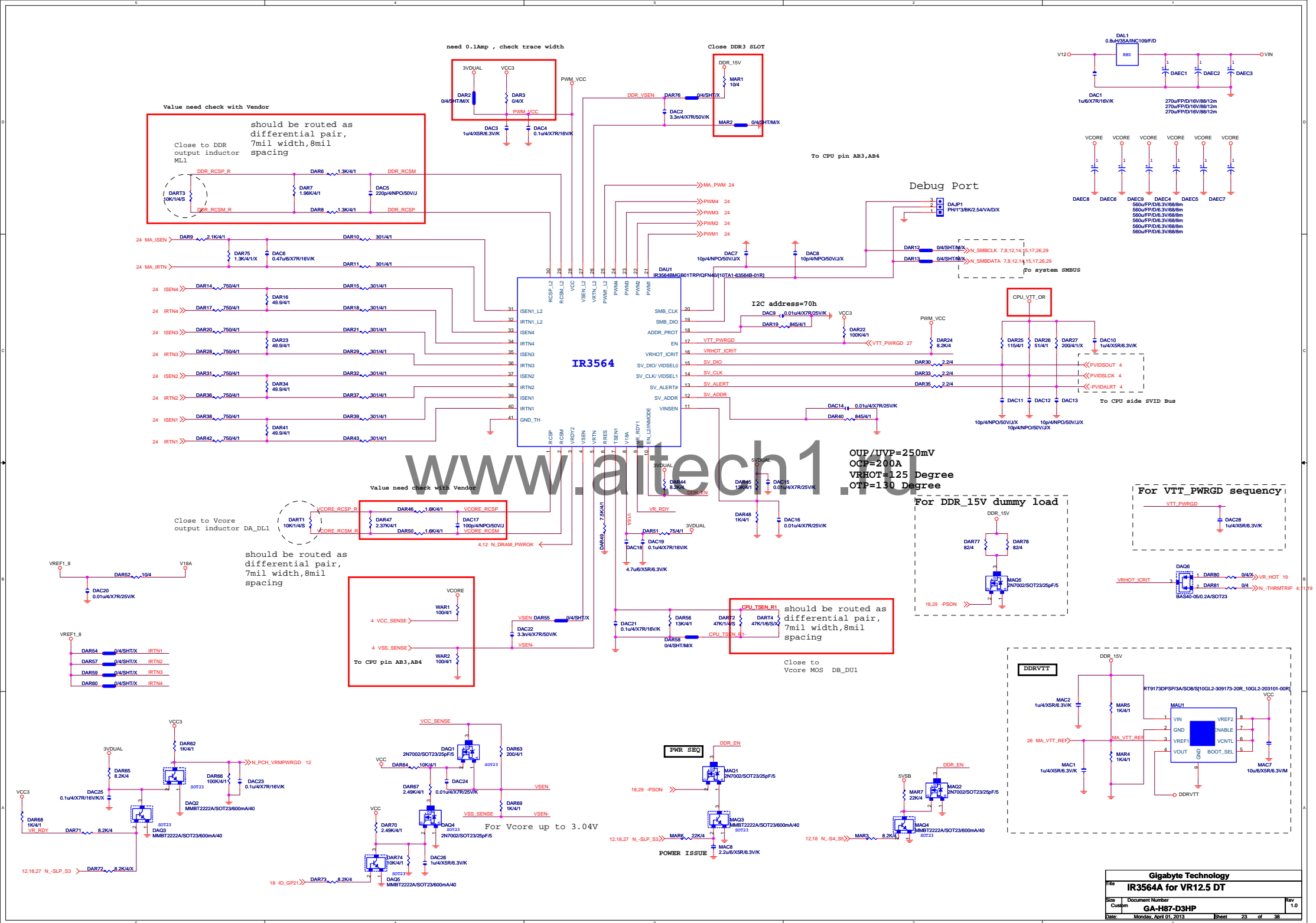
Gigabyte Technology

Title		BIOS	
Size	Document Number	GA-H87-D3HP	Rev
Customr			1.0
Date:	Wednesday, April 10, 2013	Sheet	20 of 38

	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O

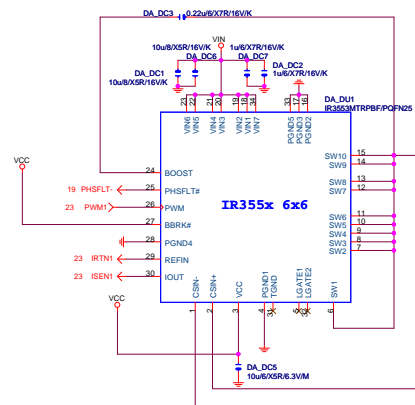




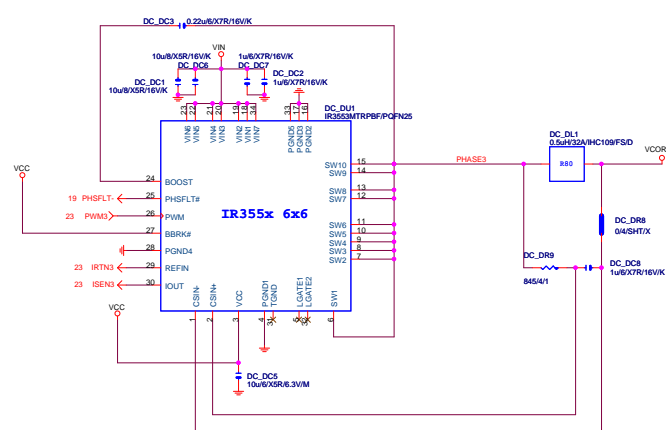


VCORE

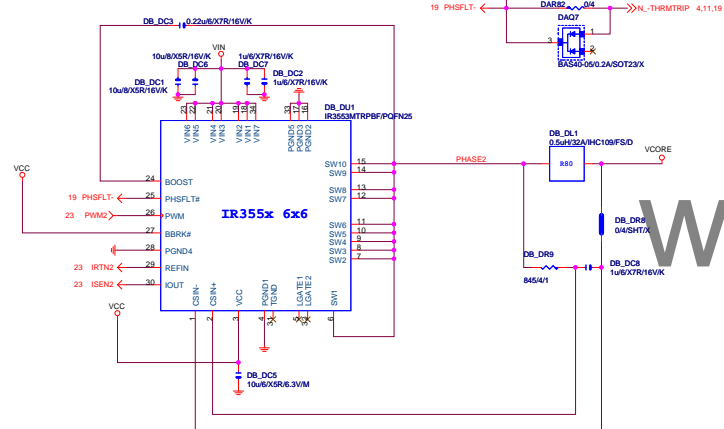
VCORE-PHASE1



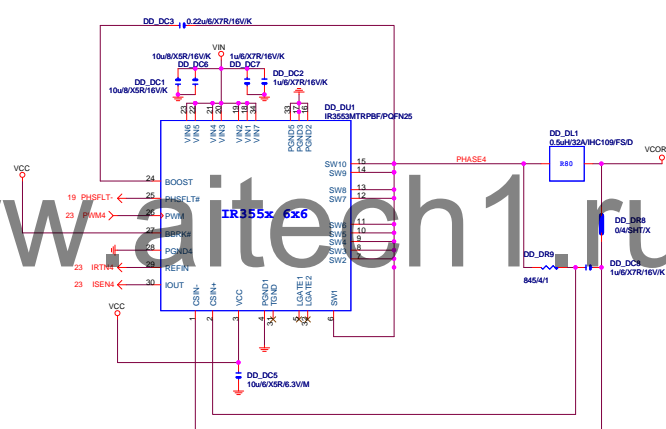
VCORE-PHASE3



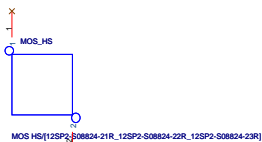
VCORE-PHASE2



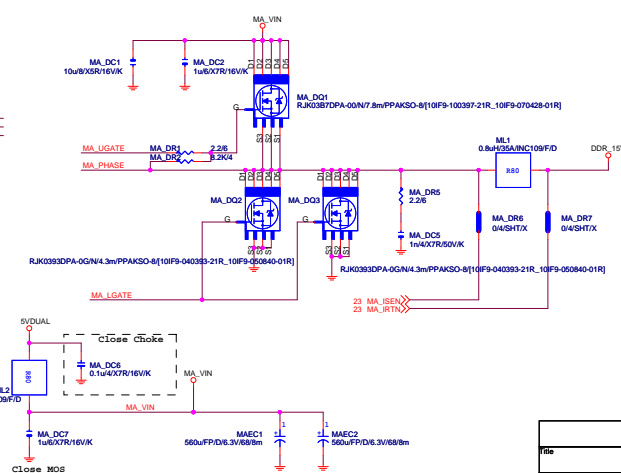
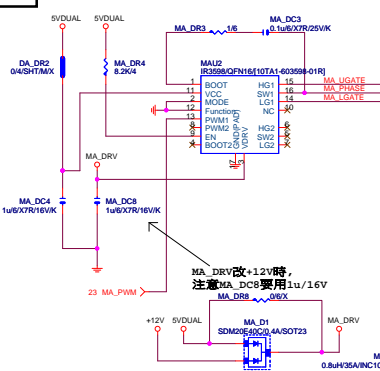
VCORE-PHASE4



MOSFET HEATSINK

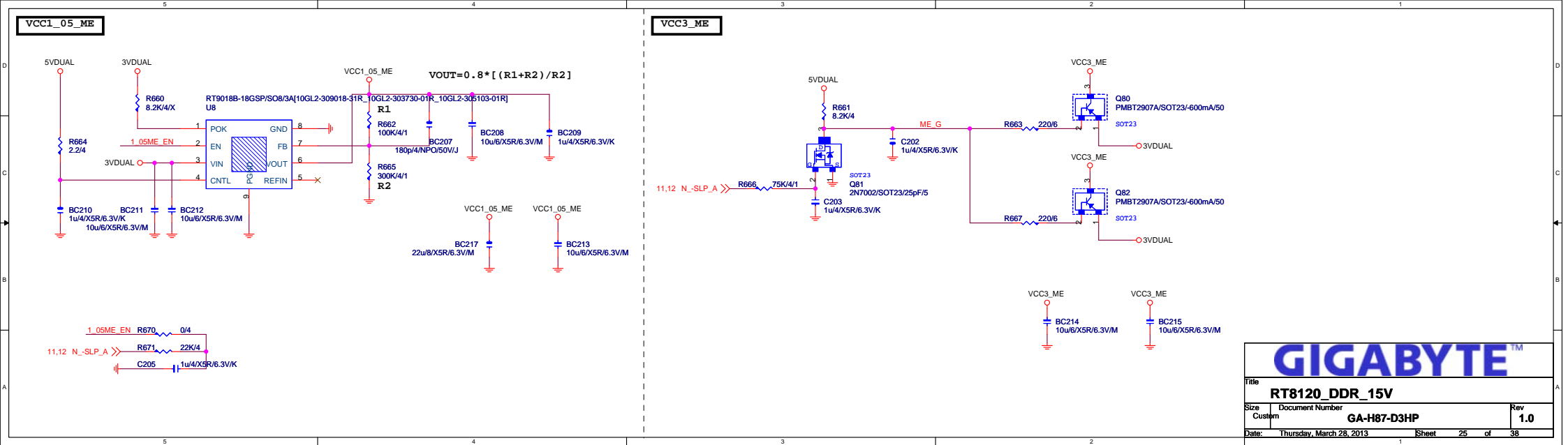


DDR_15V



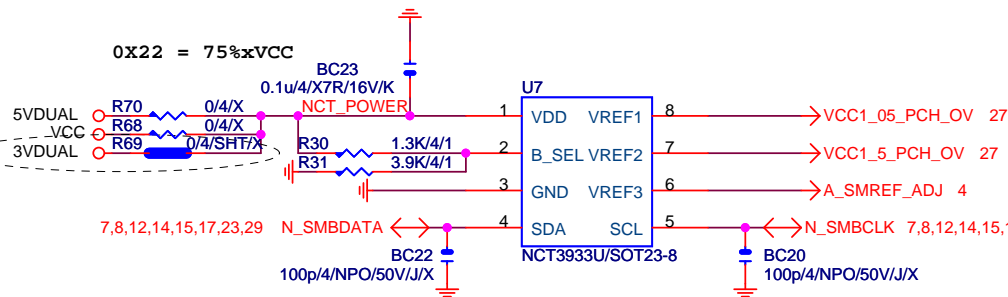
FUNCTION	MODE	PNR MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Seate	DUAL
1	0	Tri-Seate	Doubler
OPEN	0	Tri-Seate	Quad
CORN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

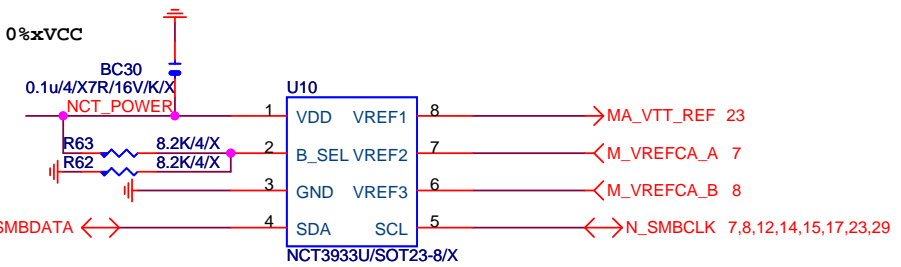


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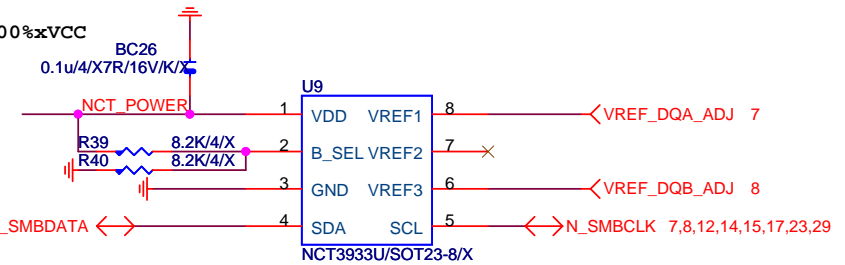
OVER VOLTAGE



0X2A = 0%xVCC



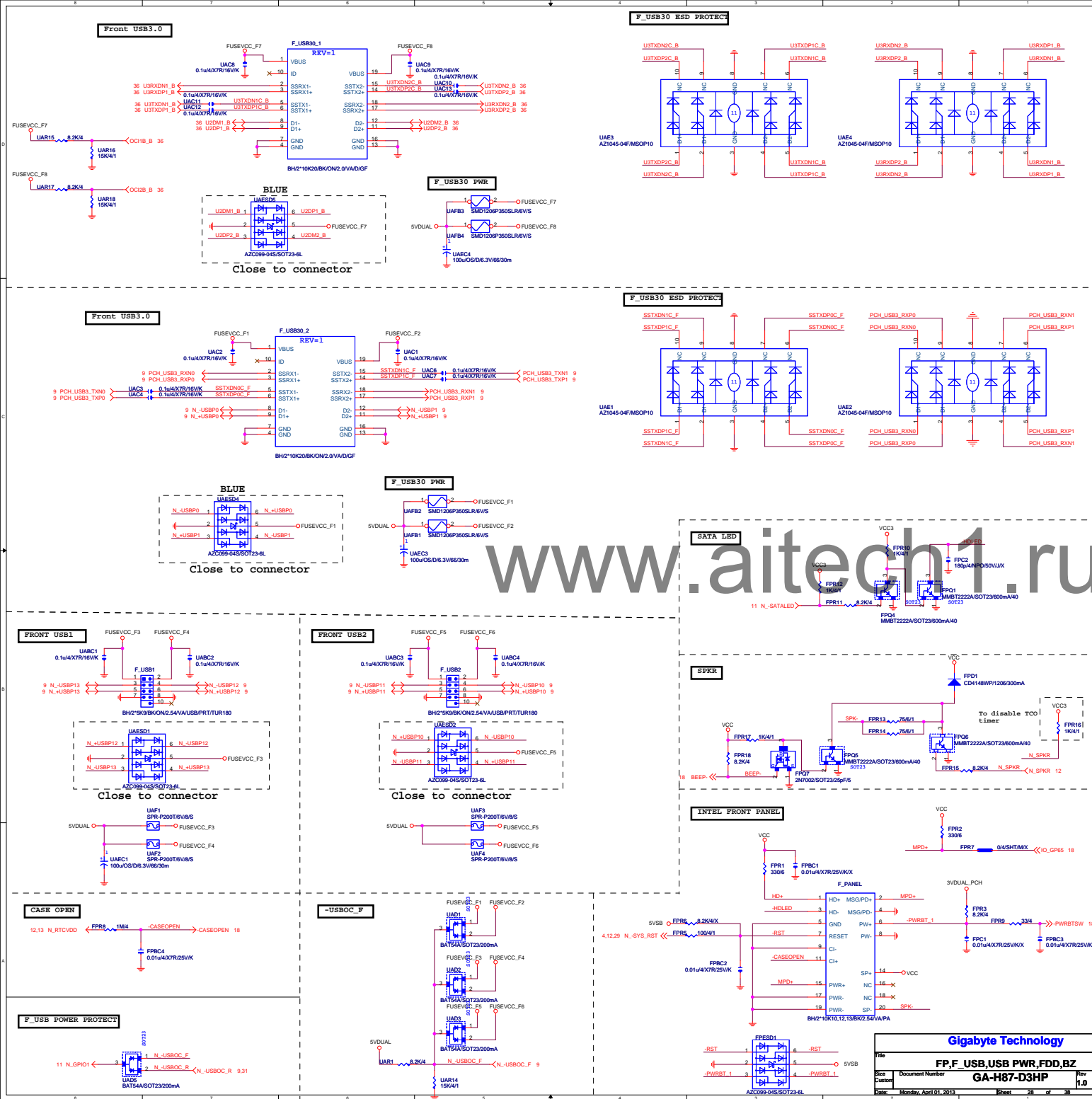
0X20 = 100%xVCC



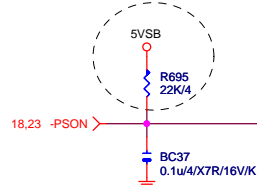
NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology

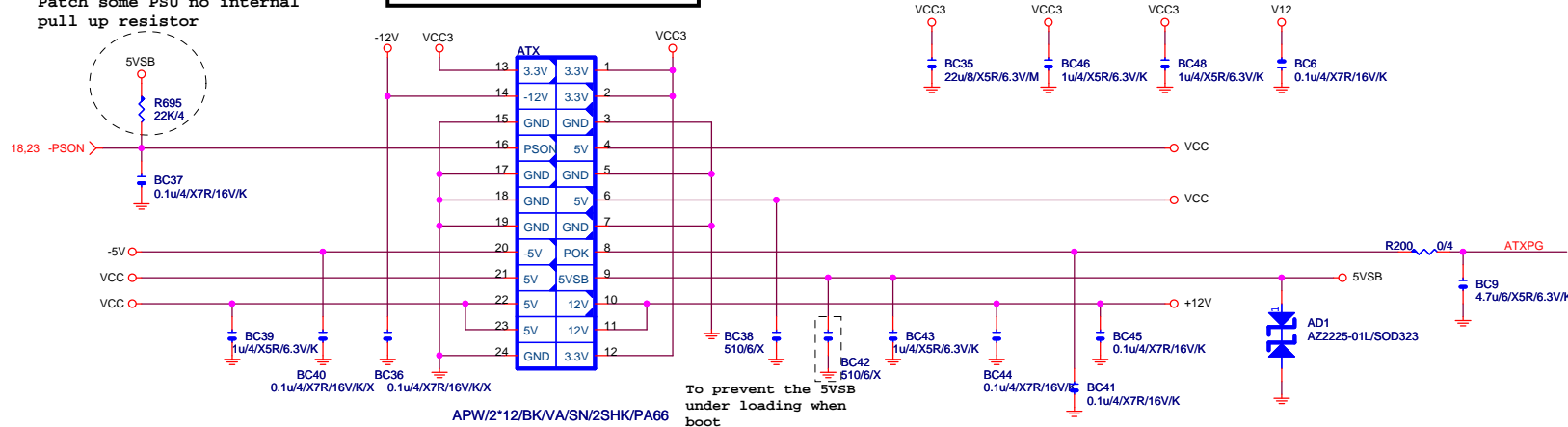
Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-H87-D3HP	1.0
Date:	Monday, April 01, 2013	Sheet 26 of 38



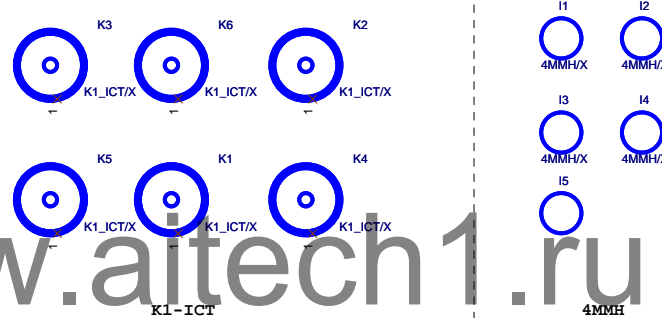
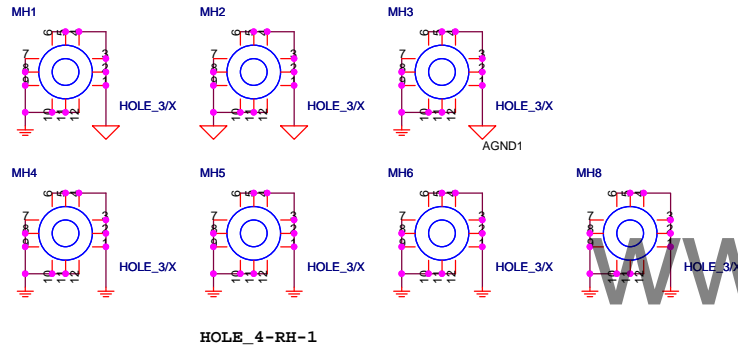
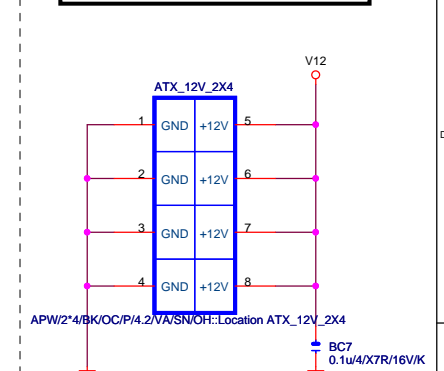
Patch some PSU no internal pull up resistor



ATXX24 POWER CONNECTOR

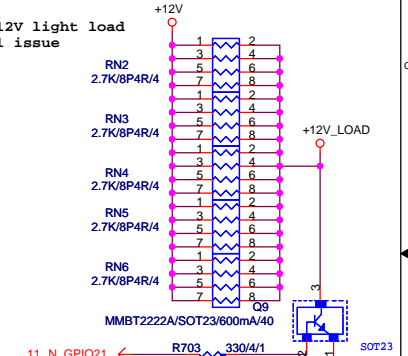


ATXX4 POWER CONNECTOR



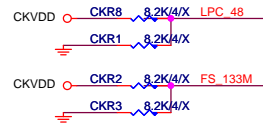
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

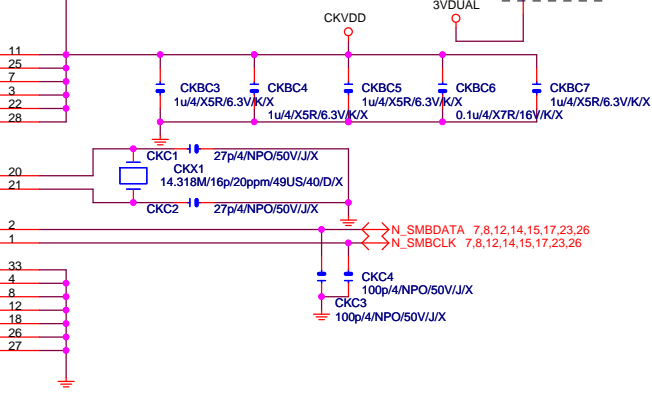
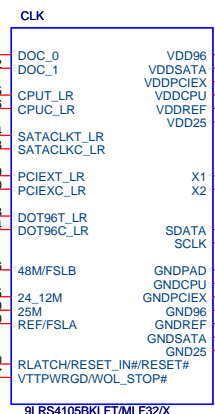
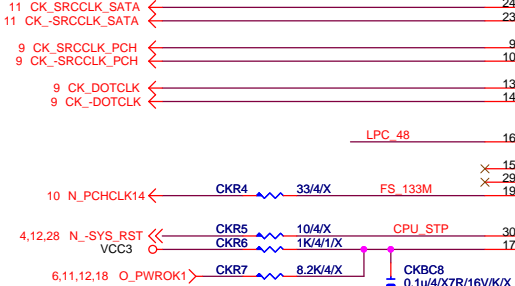


CLK GEN

CPU Frequency Selection

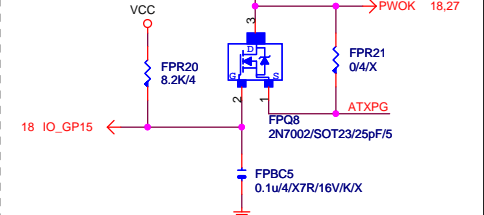


FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



PWOK PATCH

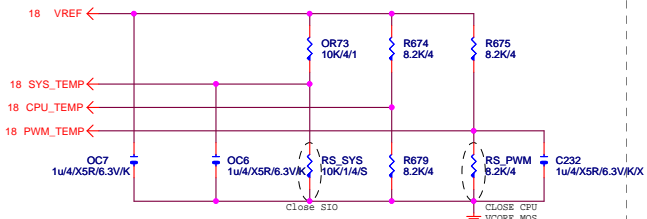
【技術通報R&D技術通報154】



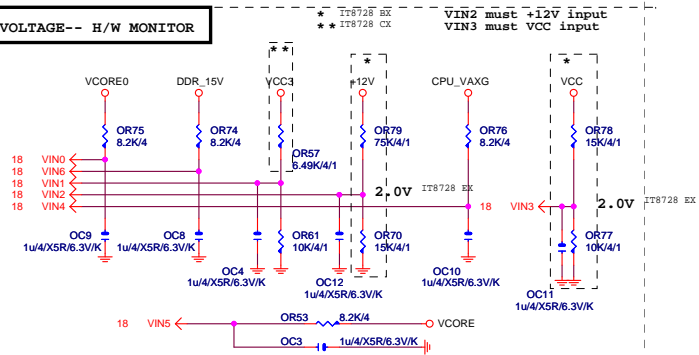
Gigabyte Technology

Title			ATX POWER CONNECTOR
Size	Document Number	GA-H87-D3HP	
Custom			
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TEMP H/W MONITOR

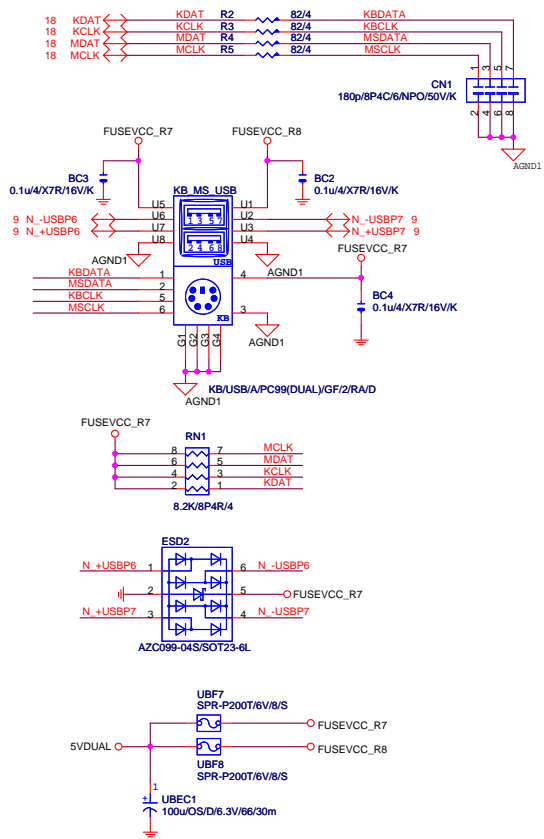


VOLTAGE-- H/W MONITOR

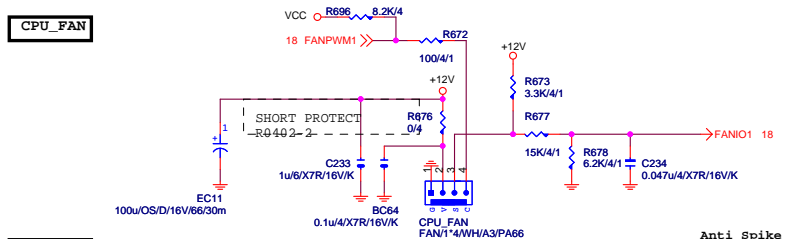


The division voltage of VIN2 & VIN3 must be around 2.9V

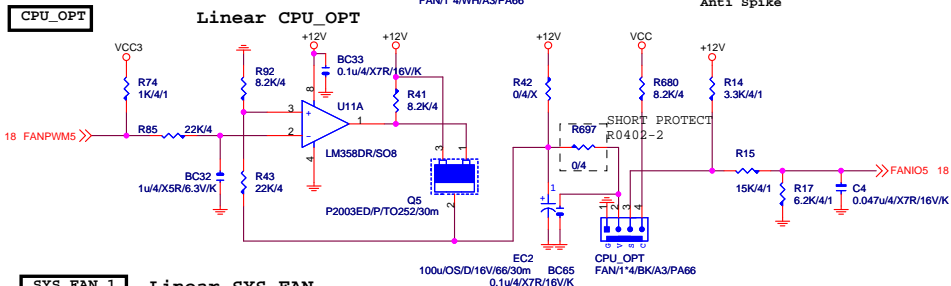
KB/USB



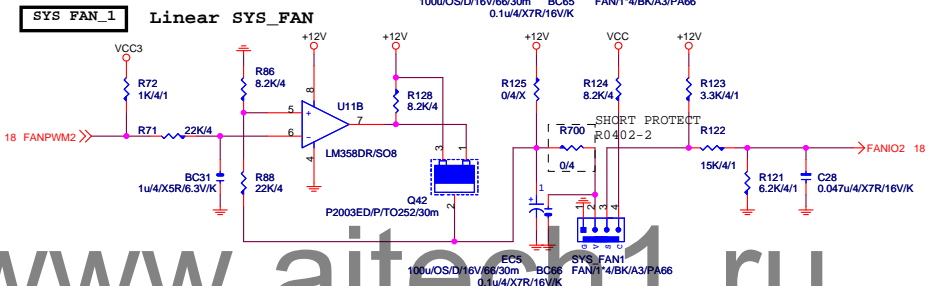
CPU_FAN



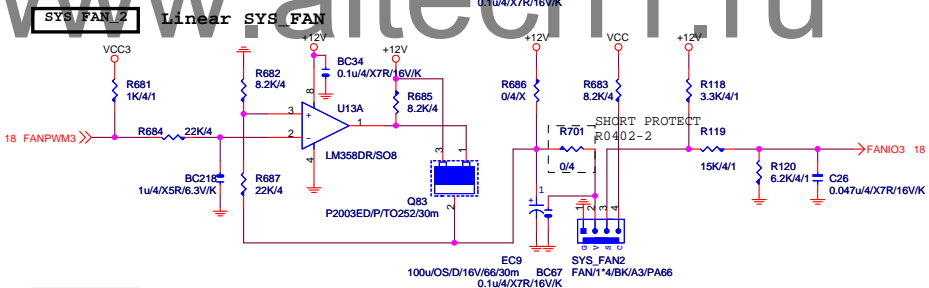
CPU_OPT



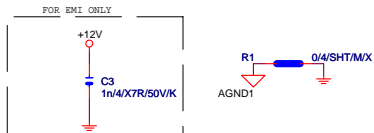
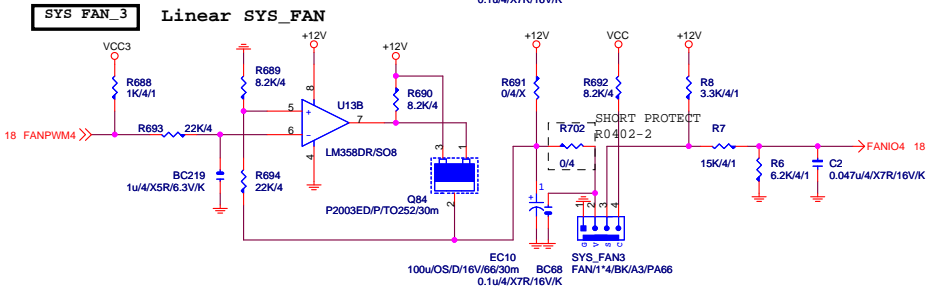
SYS_FAN_1	Linear SYS_FAN
-----------	----------------



SYS_FAN_2 Linear SYS_FAN



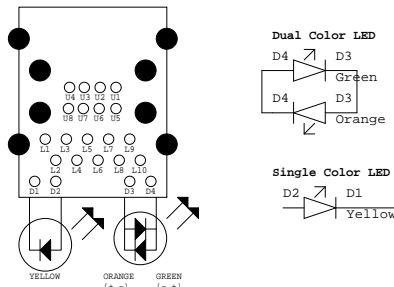
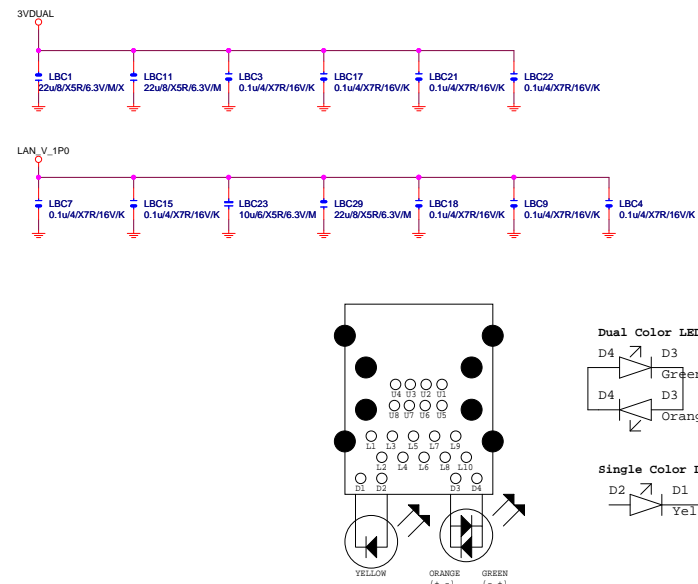
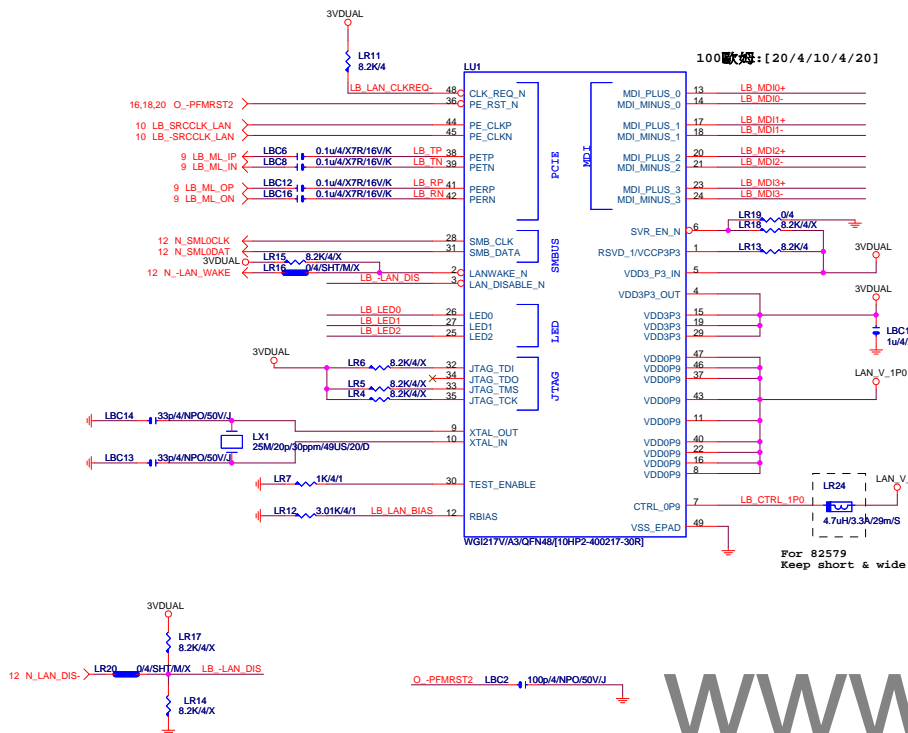
SYS_FAN_3 Linear SYS_FAN



Gigabyte Technology

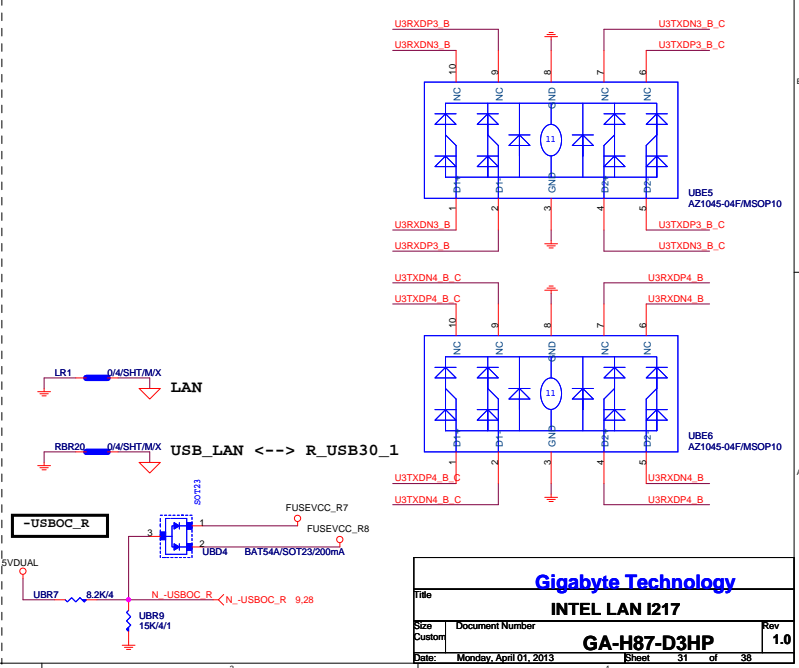
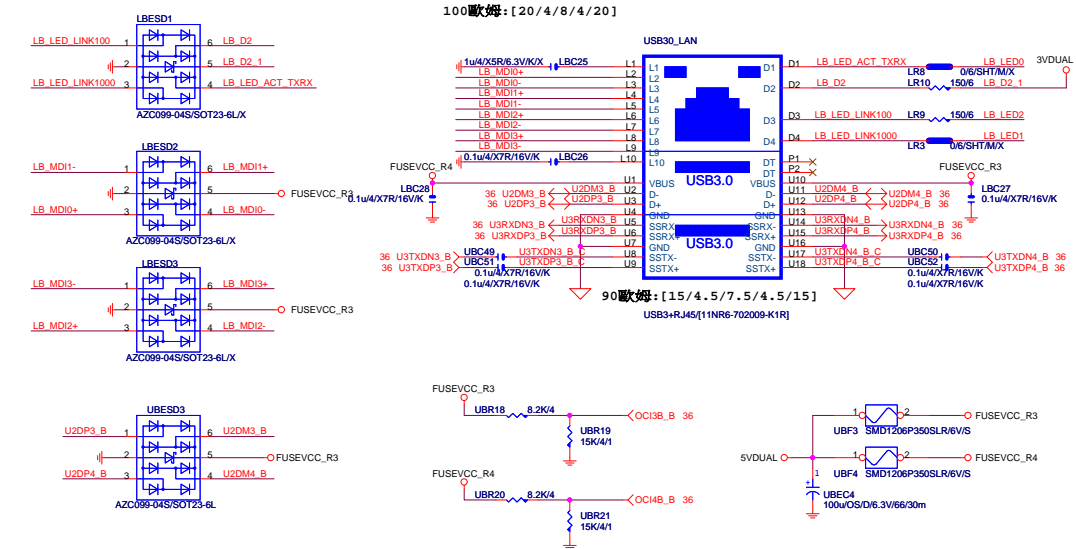
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Size		Document Number							Rev				
Custom		GA-H87-D3HP							1.0				
Date:		Monday, April 01, 2013			Sheet		30		of		38		

LAN: INTEL I217



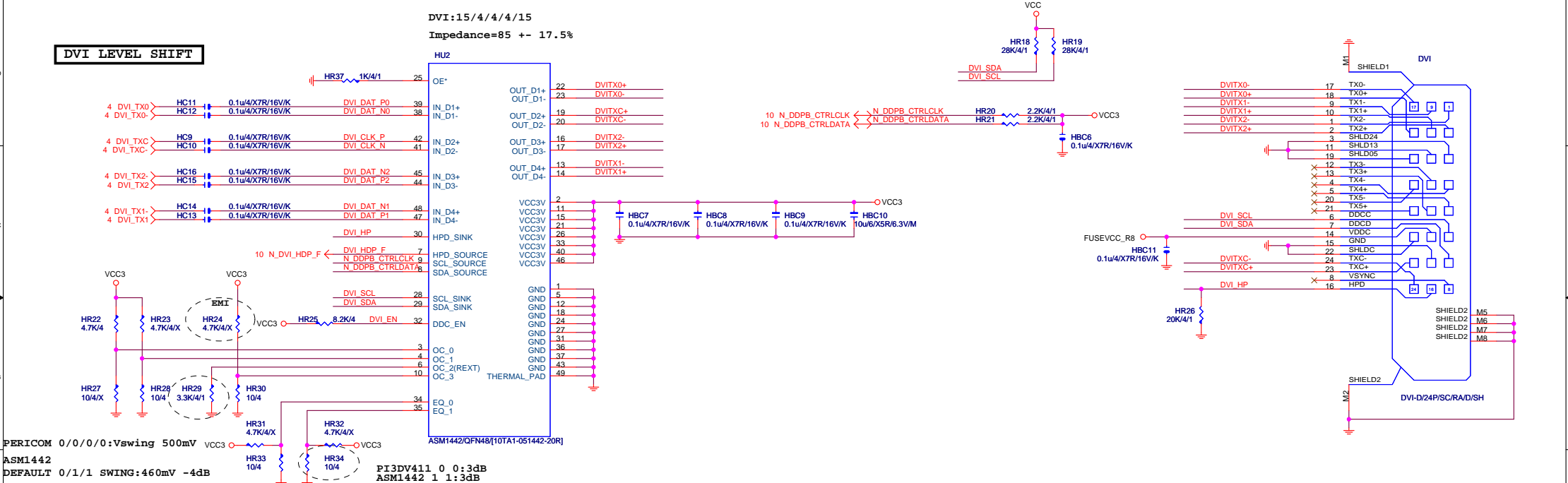
www.aitech1.ru

USB30 LAN CONNECTOR



DVI LEVEL SHIFT

DVI:15/4/4/15
Impedance=85 +- 17.5%



www.aitech1.ru

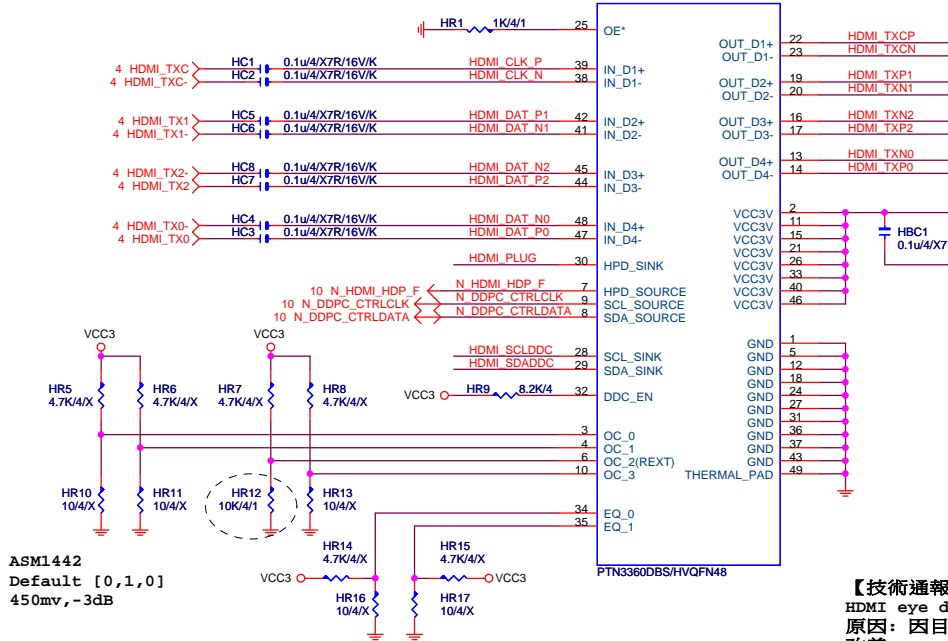
Gigabyte Technology			
TI TSB43AB23 1394			
Size Custom	Document Number	GA-H87-D3HP	
Date: Monday, April 01, 2013	Sheet	32	of 38
	Rev	1.0	

HDMI LEVEL SHIFT

HDMI:15/4/4/15

Impedance=85 +- 17.5%

HU1



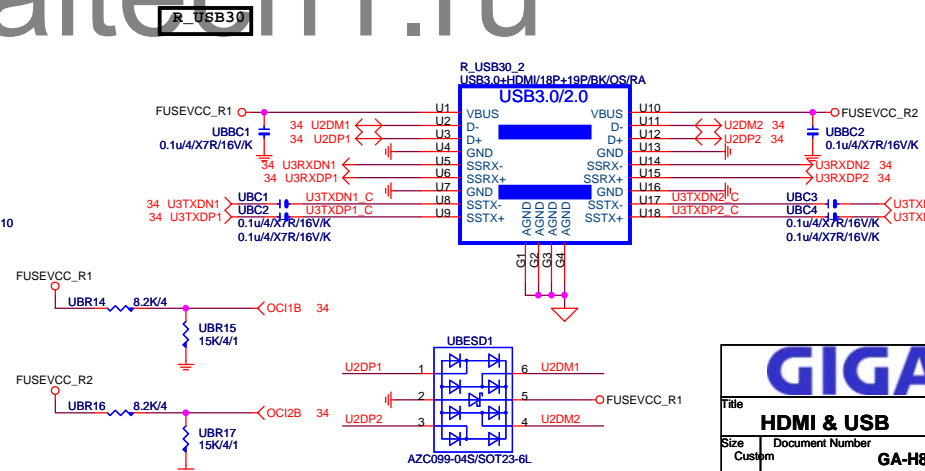
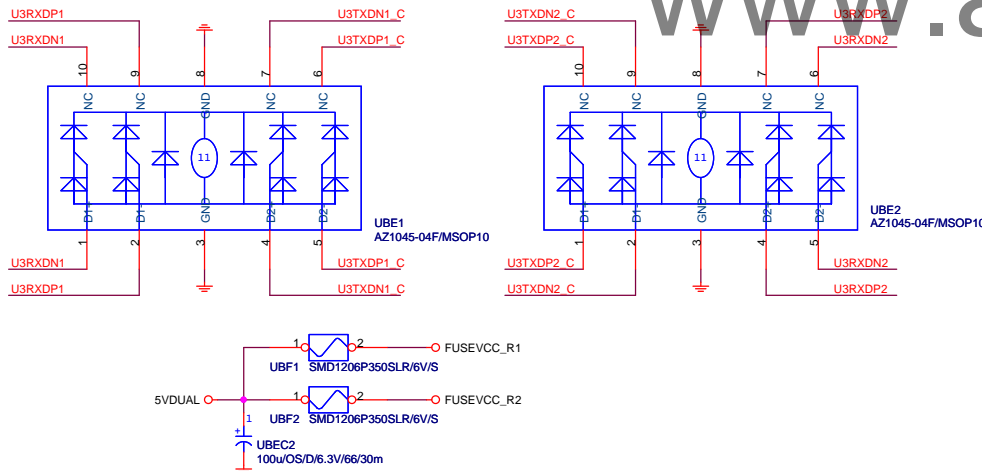
【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

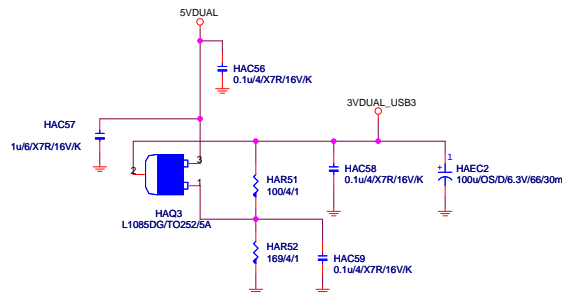
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

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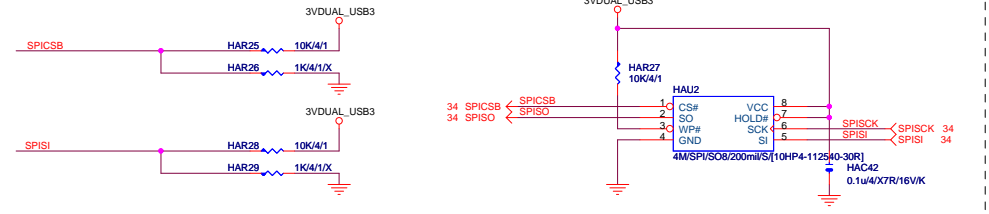


GIGABYTE™			
HDMI & USB			
File	Document Number	Rev	
	GA-H87-D3HP	1.0	
Date	Monday, April 01, 2013	Sheet	33 of 38

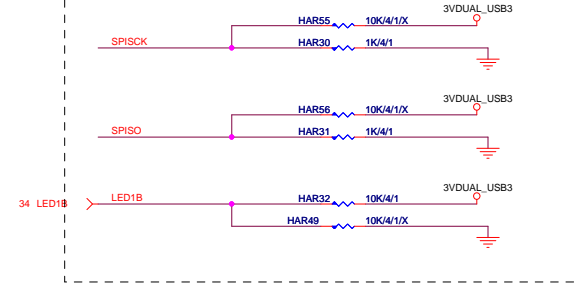
3VDUAL_USB_1



External SPI ROM ; SPI ROM attached mode

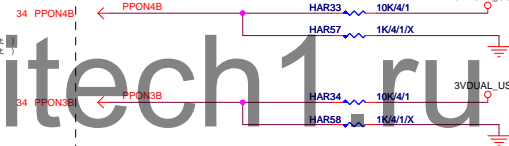


Battery Charging

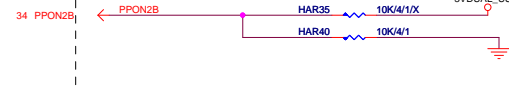


Number of Ports ; 4Ports mode

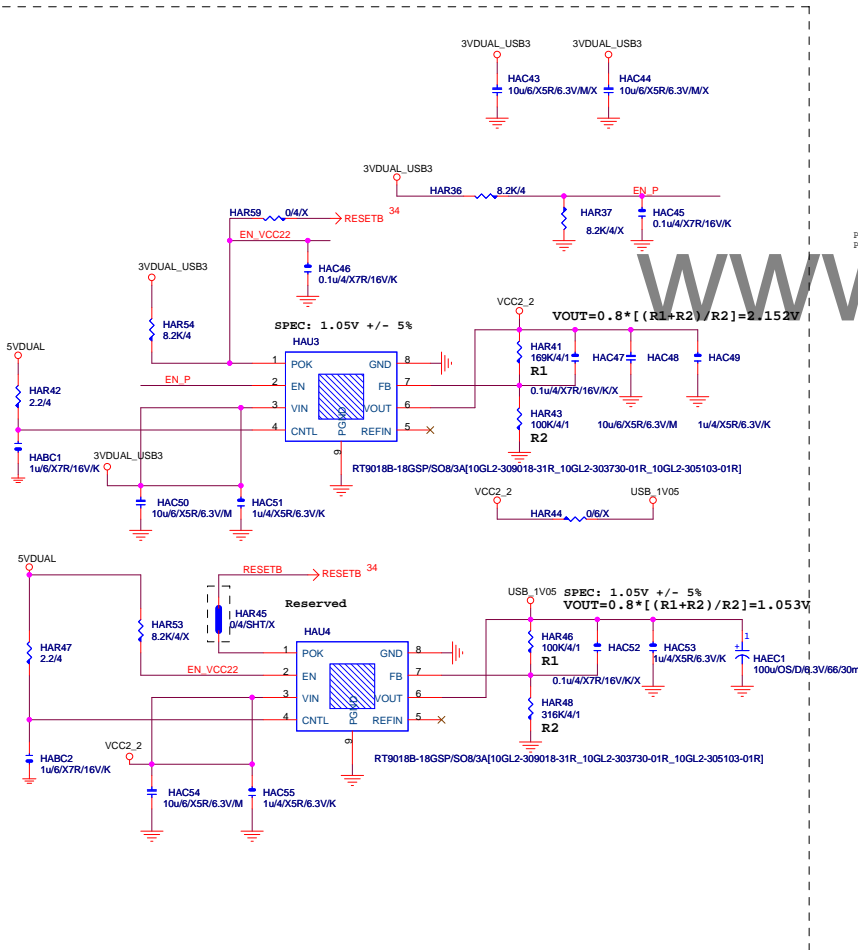
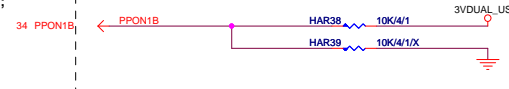
PPON3B / PPO4B : H / H (4 port)
PPON3B / PPO4B : L / L (2 port)

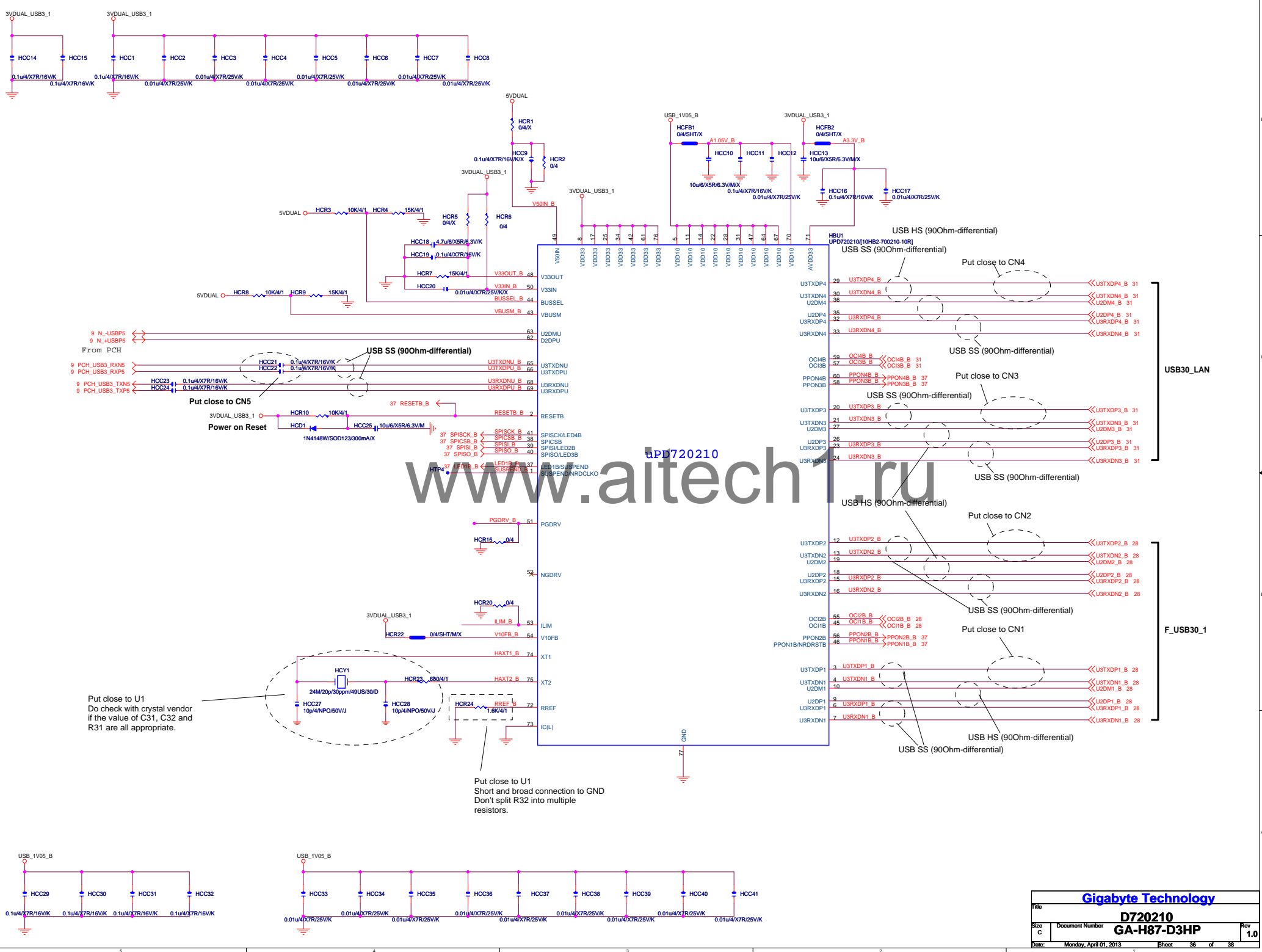


VBUS Power Control ; Individual mode

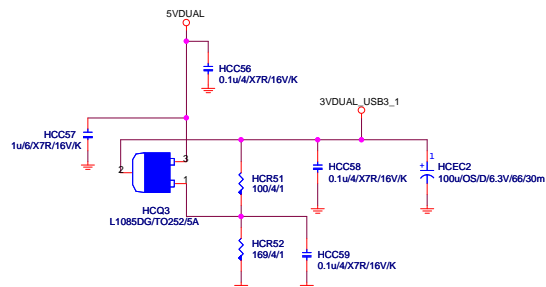


PPON1B Pin Function ; Port1 PPONB mode

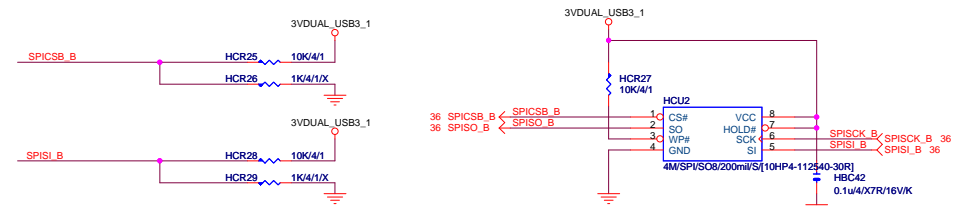




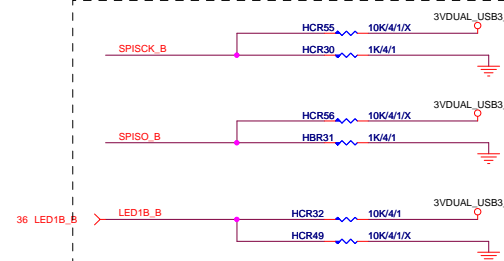
3VDUAL_USB_2



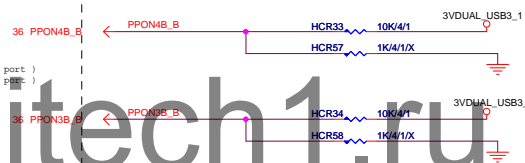
```
# External SPI ROM ; SPI ROM
attached mode
```



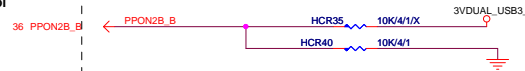
Battery Charging



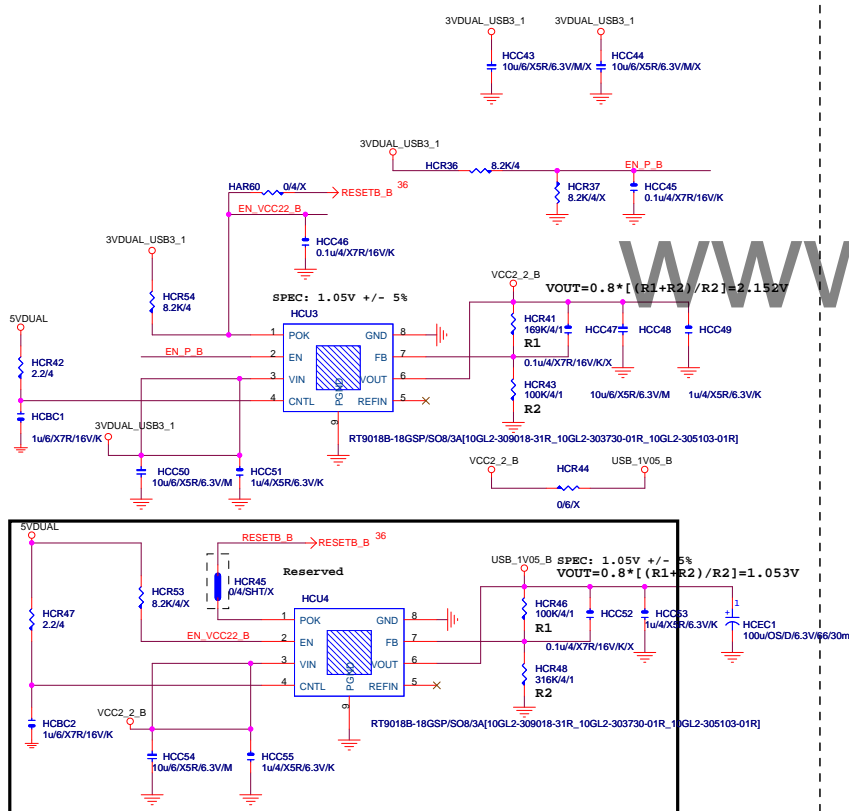
```
# Number of Ports ; 4Ports
mode
```



#5 VBUS Power Control ; Individual mode



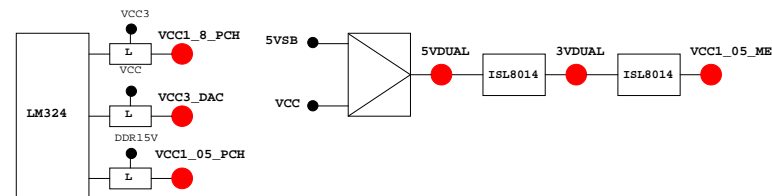
```
# PPON1B Pin Function ;
Port1 PPONB mode
```



PIN NAME	PWR	AFTER PLUG/ST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	FWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PPECI_RQT/GP14	-PPECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PPECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#C1RRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANTIO2	
FAN_TAC3/GP37	FANTIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANTIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_FWR_1	
VIDO5/GP27/SIN2	LOW_FWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	EN_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TACS/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



The diagram illustrates a 4-core system architecture. At the top, a dashed box labeled "CPU_VTT" contains a "VCORE" section with four DC/DC converters (DC_DQ1, DP_DQ1, DC_DQ2, DP_DQ2, DC_DQ3, DP_DQ3, DC_DL1, DP_DL1) and three MOSFETs (TQ3, TQ4, TL1). Below this is a "CPU SOCKET" block. To the left of the socket is a "PCH" block. To the right, a dashed box labeled "VAXX" contains a "P-PACK" section with four DC/DC converters (DZ_DQ1, DZ_DQ2, DZ_DQ3, DZ_DQ4) and three CHOKE inductors (DB_DL1, DA_DL1, DZ_DL1). The system is divided into three main sections: 1 (left), 2 (middle), and 3 (right).

```

graph TD
    subgraph CPU_VTT
        subgraph VCORE
            DC_DQ1
            DP_DQ1
            DC_DQ2
            DP_DQ2
            DC_DQ3
            DP_DQ3
            DC_DL1
            DP_DL1
        end
        MOSFET[TQ3, TQ4, TL1]
    end

    CPU_SOCKET[CPU SOCKET]

    PCH[PCH]

    subgraph VAXX
        subgraph P_PACK
            DZ_DQ1
            DZ_DQ2
            DZ_DQ3
            DZ_DQ4
        end
        CHOKE[DB_DL1, DA_DL1, DZ_DL1]
    end

    CPU_VTT --- CPU_SOCKET
    CPU_SOCKET --- PCH
    CPU_SOCKET --- VAXX
  
```

散熱模組料號:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

Z77-D3H :
PCH :
12SP2-S05511-01R/02R/03R
MOSFET :
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH